Solar Cells on CMOS Chips As Energy Harvesters

— Integration and CMOS Compatibility

Jiwu Lu

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SOLAR CELLS ON CMOS CHIPS AS ENERGY HARVESTERS — INTEGRATION AND CMOS COMPATIBILITY

DISSERTATION

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by

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This dissertation is approved by :
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“Great works are performed, not by strength, but by perseverance.”

— *Samuel Johnson*

To my dream.

CONTENTS

Chapter 1. Introduction

Energy scavenging - also known as *Energy harvesting* - has recently drawn huge interests in both academia and industry. The concept is to power micro-electronic devices by gathering energy from the environment surrounding the device itself. It is a potential solution for powering various low power electronic devices for autonomous systems; that is, maintenance free systems. In this thesis we will propose a new approach to harvest energy in a microsystem.

1.1 Why energy harvesting?

Ubiquitous computing needs hundreds of working micro-electronic devices everywhere and whenever. Traditional power supplies cannot meet the energy needs of such systems. However, the development of low-power IC technology has reach to such a level that energy harvesting from the environment surrounding the electronic device needs no longer be a dream.

Fig. 1.1 shows the envisaged ubiquitous computing system first proposed by Dr. Mark Weiser [2, 3]. He stated that: "I call this future world "ubiquitous computing"; such a world will "Provide hundreds of wireless computing devices per person per office, of all scales (from 1" displays to wall sized)."

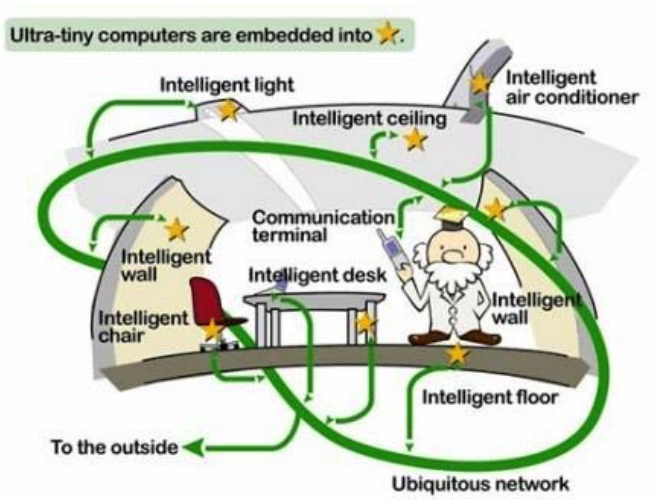

Fig. 1.1. Envisaged autonomous ubiquitous network inside an office room [1].

"A computer so imbedded, so fitting, so natural, that we use it without even thinking about it."

Although this may seem like a fantasy, ubiquitous computing will approach us in near future: during the opening plenary session of *International Electronic Device Meeting (IEDM) 2010*, Dr. Kinam Kim from Samsung declared that Samsung will develop such ubiquitous computing world before 2020.

As an essential part of merging this ubiquitous computing system with our lives, the wireless sensor network (WSN) needs to deploy many small, unnoticeable, self-sustaining sensor nodes into an environment to collect and transmit information. From now on, the term *smart dust* will be used to refer to such elementary physical devices consisting of sensors, a transceiver and supporting electronics , and which is connected to a large wireless sensor network [4].

A core challenge of such smart dust devices is to power them through out its physical lifetime (perhaps 10 years).Because the "smart dust" will be everywhere, the power supply challenge is different from existing electronic systems.

Cable wiring is the most common method of providing energy to electronic devices. But for a ubiquitous computing system, cable wiring is prohibitively expensive or even impossible in certain environments. So cable wiring is not suitable for the smart dust system.

Nowadays, batteries dominate the power supply for portable electronic devices such as mobile phones and mp3 players. There are two disadvantages: first, the energy density of the state of the art battery is still only around 1~3 kJ/cm^3 [5-7], which means a cubic-centimeter battery can provide only a few hundred days of power to a *smart dust* device consuming 100 μW; second, the self-discharge rate of the battery is 3~5% per month at 20 °C [5, 6], which means only 69.4 ~54% percent energy is left after 1 year even if the battery is not connected. Recharging or replacing these batteries by humans is therefore not a good candidate for power supply to ubiquitous systems.

The development of new batteries is slow: *the energy density of batteries has only increased by a factor of five over the last two centuries* [7, 8]. A fundamental breakthrough will be essential for the battery to satisfy the

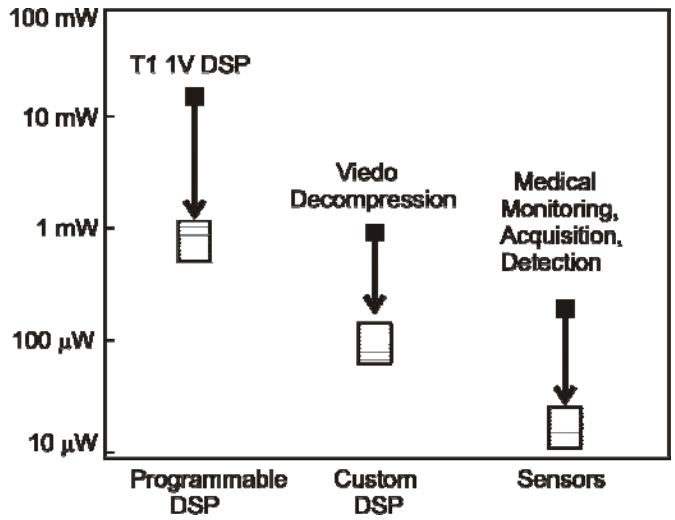

Fig. 1.2. Trends in Power consumption for low to medium throughout DSP. Modified according to [13].

demands of the fast-growing IC industry. New concepts such as the nanomaterial based battery [9], combustion-based micro-power generator [10] and micro fuel cell [11, 12], are the hopes of the future.

Advances in low-power CMOS[1] VLSI[2] have led to the dramatic decreases in power consumption. Theoretically, it was predicated that the power consumption of different motes will be below 10 µW in the foreseeable future (shown in Fig. 1.2) [13]; practically, it was reported that a CMOS image sensor can operate continuously at 70 µW/cm^2 [14] and a temperature sensor requires less than of 40 μW continuous power supply [15].

Although global warming aggravates the demand for sustainable energy, plenty of energy sources are available at a micro-scale. As reported in [16, 17] and will be discussed in detail in Section 1.3, various energy sources, such as, solar, wind and geothermal, have energy densities in the range of tens of microwatts/cm^3. All of them can provide power to the smart dust if effectively accumulated, i.e., energy harvested.

[1] CMOS: Complementary Metal Oxide Semiconductor
[2] Very Large Scale Integration

1.2 Requirements for an Energy Harvester

The energy harvester has both intrinsic requirements as an energy source and special requirements imposed by the ubiquitous computing system. In short, the energy harvester should offer **enough** power to the smart dust **everywhere** within **limited dimensions**.

1.2.1 Power

Intrinsically, the energy harvester should scavenge at least microwatts of power from the environment of the smart dust. This is because the power consumption of the smart dust is around 100 $\mu W/cm^2$, and the duty cycle is generally higher than 1%. Because there is just enough energy, and because the supply and the demand may come at different times, in practice a temporary energy buffer and power management electronics are necessary to effectively deliver the energy from the harvester to the smart dust.

1.2.2 Size

Thanks to Moore's law [18] in IC technology, the size of the smart dust is no longer the bottleneck of the system. Fig. 1.3 shows a commercially available "smart dust" including a sensor, a battery and a transceiver. The battery, which is guaranteed to have a 1-year life time, dominates both the size and the weight of the system.

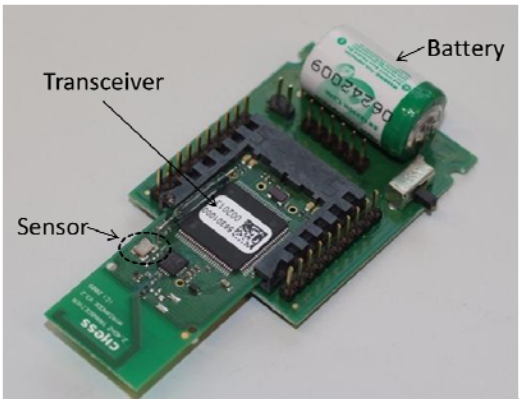

Fig. 1.3. The battery dominates the size of the sensor in a commercial available sensor node. The battery's one year life time limits the life span of this sensor node.

As the alternative to the battery, the energy harvester should not be bulky. One of the key aesthetic requirements of ubiquitous computing is that it should naturally fit into our life without being noticed.

Depending on the applications, the size of the scavenger can vary, but generally we prefer a scavenger not larger than 10 cm^3, which is a typical volume of smart dust [17]. Also it is ideal if the size of the energy harvester can scale with that of the smart dust.

1.2.3 Flexibility

The most prominent characteristic of the ubiquitous computing system is its omnipresence. So the energy harvester should also be ubiquitous. The environment of the smart dust changes according to the application, so the possible energy sources for the energy harvester also change. No simple single solution can address all applications, so the flexibility of the energy harvester will always be limited in principle. However, even the ambient of the same smart dust will have a statistical variation, and so the energy scavenger should accommodate such fluctuations. In other words, the energy harvester should have a large operating window.

The energy harvester should function typically for 10 years to be consistent with the typical physical lifetime of the electronic components in the smart dust. So the hardware of energy harvester should have excellent reliability to exploit the advantage of the infinite energy source compared to the limited energy in a battery.

1.2.4 Challenge of CMOS compatible manufacturing

One ubiquitous system needs hundreds of smart dust nodes, so the fabrication technology of the energy harvester should be suitable for commercial mass production. The energy harvester should be made of abundant and environmentally friendly materials. The process should be easy and have a good process control, which can offer high yield and small variability.

Most of the time, the energy harvester and the smart dust are fabricated separately, and they are assembled together and electrically connected. A more economically attractive approach is the integration of the energy

harvester and smart dust in a single chip. Such integration can miniaturize the power consumption, reduce the size and the total weight.

Normally the energy harvester can be realized before, between or after standard CMOS process for the chips. Adding the energy harvester after CMOS process flow (post-processing) will not influence the standard foundry process, thus the good-quality chip can be guaranteed. As detailed in Chapter 2 of this thesis, the different metal and insulator layers presented in the chip can be used as a part of the energy harvester, which is similar to the process discussed in [9]. Alternatively, like the renowned digital micro-mirrors [13], the energy harvester can be completely built on top of the CMOS chips which will be discussed in Chapter 4 and Chapter 5.

However the post-processing approach cannot be applied to processes or materials that require temperatures higher than 450 °C; the added extra layers of the energy harvester should not add too much excessive mechanical stress; chemical contamination, which will change the performance of the CMOS chips should be avoided; plasma charging damage is possible when the plasma enhanced chemical vapor deposition (PECVD) process is involved [19].

1.3 Sources for energy harvesting

There are various approaches to obtaining the "Holy Grail" for energy harvesting depending on the application. Here we discuss various energy sources from which the harvester will scavenge because this is the starting point for the design of the energy harvester.

1.3.1 Sunlight

Most energy used by human beings today - such as that from coal, gasoline, and oil - originate from sunlight. Sunlight is also the best choice for the energy harvester if it is available.

The average power density of outdoor sunlight is 100 mW/cm^2 under AM 1.5 illumination spectrum [20] and that of an indoor light may vary widely, typically from 0.1 to 1 mW/cm^2, depending on e.g. the type and the position of the light source [17].

The obvious device to harvest solar energy for electric means is the photovoltaic (PV) cell, also known as solar cell. With a history of more than 50 years, there are various solar cell technologies [21]. Most have an outdoor photovoltaic (PV) efficiency more than 10% [22] and some solar cells have a good performance (more than 5%) even under weak light illumination such as indoor light [23, 24]. So if the outdoor light is available, the solar cell energy harvester can offer more than 10 mW/cm^2 output; for indoor light, some solar cells can still offer microwatts per square centimeter, which still meets the requirement for the energy harvester.

The reliability of solar cells is very good: off-the-shelf solar cells often come with a 20 years guarantee. The voltage output of the solar cell is almost constant under different illumination, so the operating window of the energy harvester based on light is also very large.

However, if there is no light available at all, for example, a pressure sensor system inside a car tyre, the use of PV harvester is not an option.

1.3.2 Mechanical Vibrations

In nature, low-level mechanical vibrations can be found in many places, such as computer fans and microwave ovens. High-level mechanical vibrations are available from devices such as a car engine and the blades of a helicopter.

There are two important factors playing a role in a possible energy source for mechanical harvesting: the displacement and the acceleration amplitude (A) that can be induced by the source. In [16], Shad Roundy et al., showed that there are two common characteristics for all the low-level vibration sources: the displacement is greatest somewhere below 200 Hz, and the acceleration amplitude magnitude spectrum is relatively independent on frequency (ω). The vibration amplitude is generally in the range of 5~20 μm [16]. Information about the vibration sources is essential to the design of vibration harvesters. As shown in [16], the energy harvester should be designed to resonate at the fundamental vibration frequency, because the maximum energy output drops rapidly with increasing mismatch between resonant frequency and stimulation frequency (see Section 2.1).

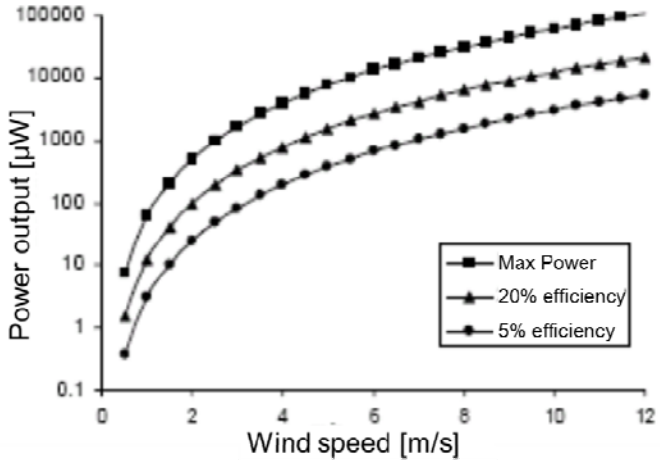

Fig. 1.4. Power density from Air flow at different wind speed and different efficiency modified according to [17].

Scavenging mechanical vibration power dominates the research community over recent years, and will be discussed in more detail in Chapter 2.

1.3.3 Air flow

Air flow is widespread, and people began to harvest wind energy more than 4000 years ago for sailing. Windmills also helped Dutch people to pump water from low-lying land into the sea. Wind power will be one of the primary green energy sources for the energy-starving world [25].

As an energy source for "smart dust", on first sight wind energy meets the requirements of the energy harvester quite well. Fig. 1.4 shows the possible energy densities versus the wind speed at three different conversion efficiencies. A power output of 100 $\mu W/cm^2$ is a realistic target even with an efficiency of just 5% at wind speed of 5 m/s.

There are reports about airflow harvesters based on the wind turbine [26-28]. Although they report promising energy output, they are relatively large devices that are incompatible with the size of the smart dust and thus unsuitable for most WSN systems. It is reported, a micro windmill of 1 cm^3 can generate 1 mW power at a wind speed of 40 m/s [29], and this low conversion efficiency is probably due to the relatively high viscous drag on the blades when the turbines are miniaturized [30].

1.3.4 Thermal Gradient

There will be a potential difference between two dissimilar metal conductors depending on the junction temperature of these two conductors. This is the so-called Seebeck effect, and is the physical principle of a thermoelectric generator. In ambient air, there are naturally occurring temperature gradients that can provide an energy source for energy harvesting. The maximum efficiency η of such a thermoelectric generator is given by the Carnot's theorem [31, 32]:

$$\eta = \frac{T_{High} - T_{Low}}{T_{High}} = \frac{\Delta T}{T_{High}} \tag{1.1}$$

The practical efficiency is only about 10% of the theoretical maximum. For a temperature difference of 10 °C, at room temperature the maximum power output is generally less than 50 μW/cm^2 [33], which is quite high compared to the alternatives.

Research has been carried out on small-scale thermoelectric energy harvesters [34-37]. Also, there are commercial thermoelectric products such as the Seiko Thermic watch.

1.3.5 Human Power

From resting to running, the human body burns 0.1~1.5 kW. An average human body burns about 10.5 MJ of energy per day, and it corresponds to an average power dissipation of 121W [38]. Human power sources are classified into passive and active sources: the active ones require humans to constantly perform in action such as shaking and cranking; the passive ones don't require humans to do anything extra to generate power. The latter is preferred for ubiquitous computing. Fig. 1.5 shows an energy harvesting shoe, which scavenging energy from human walking.

There are experimental reports of harvesting power from human walking [39-41]. The MIT group [38] showed that a piezoelectric shoe is capable of producing an average power of 330 microwatts per cubic centimeter. There are also commercially available self-winding watches powered by the kinetic energy of a swinging arm. In [42, 43], Mitcheson et al. presented a detailed

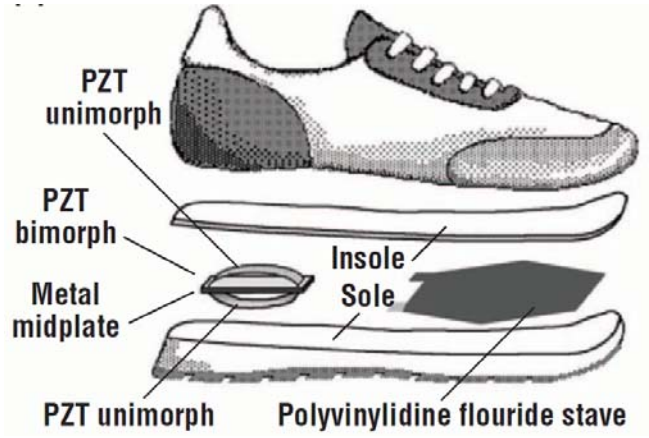

Fig. 1.5. Energy harvester that scavenges the energy from human walking [8].

analysis about the optimization of the energy harvester based on human motion.

1.3.6 Radiofrequency (RF) radiation

The RF spectrum is a part of the electromagnetic (EM) spectrum, and ranges from 3 kHz to 300 GHz. The energy density of the electric field of a plane EM wave is $\frac{\varepsilon}{2}|E_0|^2$, where ε is the permittivity of the medium and E_0 is the electric field strength [44]. For far-field application, which is case in our application, E_0 is inversely proportional to the distance from the source of the radiation.

The biggest advantage of RF radiation is its abundance. Radio, television broadcasts, mobile telephone services and wireless local area network (WLAN) cover every urban region, which makes RF radiation so pervasive that it fits the concept of ubiquitous computing well. The other advantage is that the energy harvester for RF radiation can be integrated into the micro-electronic device [45], so by the standard CMOS process flow, the flexibility and the reliability are no longer a problem.

However, the disadvantage is that the power level of RF radiation is lower than that of the other sources. There is a maximum permissible human exposure (MPE) to RF radiation due to health concern. The International Commission on Nonionizing Radiation Protection (ICNIRP) [46] and IEEE

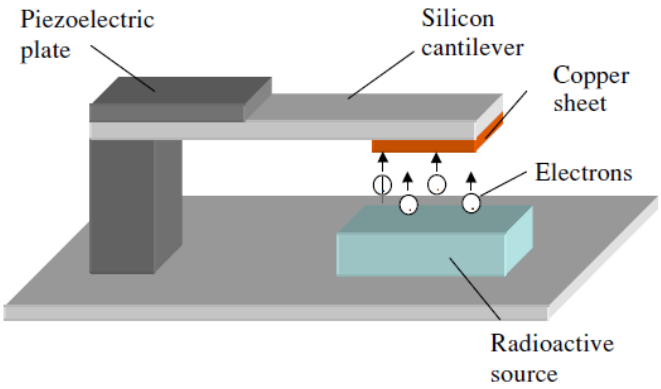

Fig. 1.6. Energy harvester based on radioisotope [54].

[47] both recommend that MPE should not exceed 1-5 mW/cm^2. Due to the typical long distance from the RF source, RF Power is normally orders of magnitude smaller than 1 mW/cm^2 in most places; generally less than 10 μW/cm^2 [48, 49].

If the RF radiation source is close to the smart dust, RF radiation harvesting is successful with the involvement of the human activity such as pushing the button of sending signal [45, 50, 51]. For the RF radiation energy harvester the design of the antenna is important [52], and the size of the antenna prefers to be larger than the wavelength of the RF radiation [53].

1.3.7 Radioisotope

When a radioisotope atom decays into a more stable one, it releases certain particles that have certain amount of energy. It is possible to harness the energy released by this decay process, but with a relatively low conversion efficiency [55, 56].

Fig. 1.6 shows the principle: the electron released from the radioactive source electrostatically charge the copper sheet, thus the electrostatic field will increase. The beam will be attracted downwards, until it touches the source. Upon touchdown the electrons in the copper sheet will be neutralized by the conductive radioactive source, thus the beam is released to vibrate at its resonant frequency, allowing energy harvesting from the piezoelectric plate.

Table 1.1. Comparison between (presumably CMOS-compatible) energy harvesters.

Harvester	Reference	area (mm2)	power/area (μW/mm2)	Requirements
solar cell, outdoor	Green [22]*	\	50-200	AM1.5 (sunlight)
solar cell, indoor	Van Veen [59] Reich [24]	\	0.01~1	Indoor lighting, 1-10 W/m2
Piezoelectric	Elfrink[60]	49	0.49	Good frequency match required
Electromagnetic	Jones [61]	99	0.37	
Electrostatic	Arakawa [62]	400	0.015	
Thermo-electric	Böttner [37]	1.12	0.6	Gradient > 5 ºC
Micro-windmill	Holmes [29]	113	0.02	5 m/s wind speed

*: There are more than 10 types of solar cells, and they have different efficiencies. Here only a range is given.

One advantage of a radioisotope energy generator is that radioactive materials can provide extremely high energy densities and over extremely long life time. However, the key disadvantage is that the use of radioactive material can be a serious health hazard and is therefore highly controversial.

1.4 Advantage of a solar cell as an energy harvester

From aforementioned sections, we know that energy harvesting is promising for smart dusts of ubiquitous computing systems, and there are many approaches based on different energy sources.

A comparison of energy harvesting techniques is presented in Table 1.1. The table is limited to approaches which are likely CMOS-compatible. This compatibility allows a high level of integration, a prerequisite for low cost mass fabrication. For the energy harvesters using mechanical vibration, only those matching general vibration sources [57] are included. The performance comparison is made per surface area (as in [58]), because CMOS power consumption scales with chip area. The table makes clear that solar cells can provide competitive power levels, even indoor. In addition, ac to dc conversion is required for most alternatives, but not for photovoltaics (PV).

On the size scale of microchips, thin-film solar cells can be considered to have the most mature of the technologies among those listed in Table 1.1. They offer both long-term reliability (> 20 years) and low-cost mass-production. From the system perspective, their merits include the delivery of

dc power and an output voltage hardly dependent on the illumination intensity. Last but not least, the photovoltaic (PV) power generation will scale with chip area, just like a chip's power consumption. So solar cell as an energy harvester is a good choice for a smart dust, but on-CMOS chip solar cells as energy harvesters have not been explored yet.

1.5 Outline of the thesis

In this thesis, two types of energy harvesters on top of the CMOS chips are presented.

Chapter 2 discusses the energy harvester based on mechanical vibrations. After a general mathematical model for the vibration based energy harvester, three main-stream types of vibration-based energy harvester will be described. Then a schematical design of our energy harvester will be given, and results of the modeling of this device are also given. Finally, the challenges of the vibration-based generator are presented.

Chapters 3~5 are devoted to using two types of solar cells as for energy harvesting: the amorphous silicon solar cells (a-Si) and the copper indium gallium (di)selenide (CIGS) solar cells. Chapter 3 describes the motivation of the monolithic solar cell integration on top of a CMOS chip, the selection of the solar cell technology and the types of CMOS chips that used. Then the influence of the passivation layer on CMOS performance will be given. Chapter 4 deals with integration of the amorphous silicon (a-Si) solar cells, and chapter 5 deals with the integration of the CIGS solar cells.

Final conclusions and future recommendations are given in Chapter 6.

Chapter 2. Vibration based energy harvester

As described in Section 1.3.2, mechanical vibrations were quickly acknowledged as the most ubiquitous energy source, thus it has received intensive research attention in the past. In this chapter, more details about the vibration-based energy harvester will be given along with a modeling study of an integrated electromagnetic based generator.

2.1 General model for vibration conversion

A vibration based power generator for an energy harvester is typically based on a mass-spring structure enclosed in a frame as shown in Fig. 2.1. Acceleration applied to the frame is coupled to the mass only by the spring, and results in a change to, generally an increase in, the spring's potential mechanical energy. A mechanical-to-electrical converter then transforms the stored mechanical energy into electrical energy.

A simple but practical model based on Fig. 2.1 was proposed by William and Yates in [63]. They used Eq. (2.1) to describe the kinematic behavior of the energy harvester, and based on that they obtained the generated power as described by Eq. (2.2).

$$m\ddot{z} + c\dot{z} + kz = -m\ddot{y} \tag{2.1}$$

where z is the spring deflection, y is the frame displacement, m is the proof mass, c is the damping coefficient, k is the spring constant.

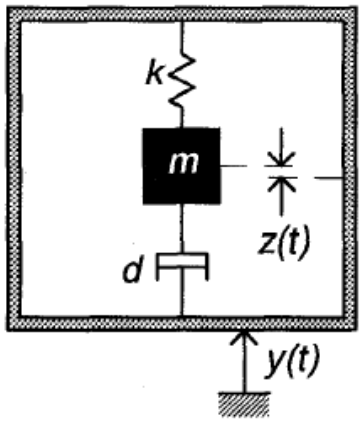

Fig. 2.1. Schematic diagram of the vibration based generator [63].

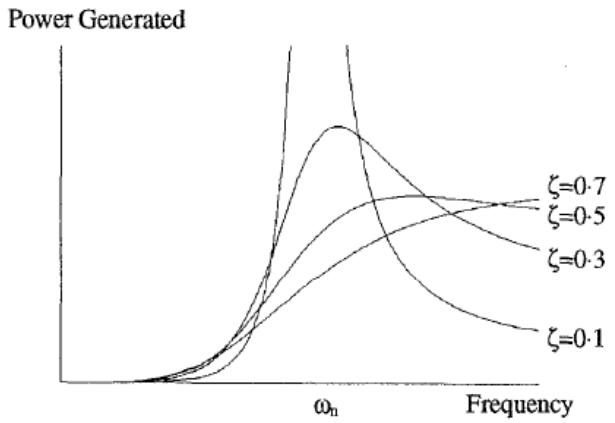

Fig. 2.2. Frequency spectrum of power generation around the resonant frequency of the mass-spring system for different damping factors [63].

$$P = \frac{m\zeta Y_0^2 \left(\frac{\omega}{\omega_n}\right)\omega^3}{\left[1-\left(\frac{\omega}{\omega_n}\right)^2\right]^2 + \left[2\zeta\frac{\omega}{\omega_n}\right]^2} \tag{2.2}$$

where P is the power output, ζ is the damping ratio, ω is the frequency of energy sources, ω_n is the resonant angular frequency of the energy harvester, Y_0 is the amplitude of the vibration source.

If the resonant frequency of the mass-spring system matches the frequency of the energy source, i.e., $\omega = \omega_n$, Eq. (2.2) can be reduced to Eq. (2.3) and Eq. (2.4).

$$P = \frac{mY_0^2\omega^3}{4\zeta^2} \tag{2.3}$$

$$P = \frac{m\zeta(\omega^2 Y_0)^2}{4\zeta^2\omega} = \frac{mA_0^2}{4\zeta\omega} \tag{2.4}$$

where $A_0 = \omega^2 Y_0$ is the acceleration amplitude.

From Eq. (2.2), we can plot the possible power output from energy harvesters with different damping ratio versus the resonant frequency of the vibration source (Fig. 2.2).

From the Eq. (2.2) and Fig. 2.2, we can make the following design rules for the energy harvester for maximum power generation:

a) The proof mass should be as heavy as possible within the size allowed.

b) The resonant frequency of the energy harvester should match the frequency of the energy source as much as possible.
c) The mechanical damping should be small.

From Eq. (2.3) and Eq. (2.4), we can make the following selection rules for vibrational energy sources, if there are multiple vibration sources available:

a) If the frequencies of the vibration sources, ω, are similar, find a place where the vibration amplitude Y_0 is the maximum.
b) If the acceleration amplitudes, A_0, are on the same level, the vibration that has a lower frequency, ω, is preferred.

2.2 Types of vibration based energy harvester

At the beginning of the energy harvesting era [57, 63], three types of vibration-based energy harvesters were developed worldwide, categorized by the conversion mechanism from kinetic energy to electricity. These will be discussed in the following subsections.

2.2.1 Electromagnetic energy harvester (EM harvester)

An electromagnetic generator is a micro-scale dynamo, which utilizes Faraday's law, i.e., a voltage is "induced" in a coil when the coil moves relatively to a magnetic field. The relative movements are caused by the mechanical vibrations (See Fig. 2.3).

The biggest advantage of the electromagnetic generator is that: if the energy harvesters have the same size, it can, theoretically, provide the largest possible power output [17]. The practical realization is rather simple [13, 61, 63]. When miniaturized, the resonant frequency of the EM harvester can match the frequency (below 200 Hz [16]) of the low level vibration sources [61, 64-66].

A disadvantage is that with the scaling down of the size, the output voltage of electromagnetic generators are alternative and small, generally smaller than 0.2 V, so a transformer will be needed. Another disadvantage is that the monolithic integration of a permanent magnet is difficult [67, 68].

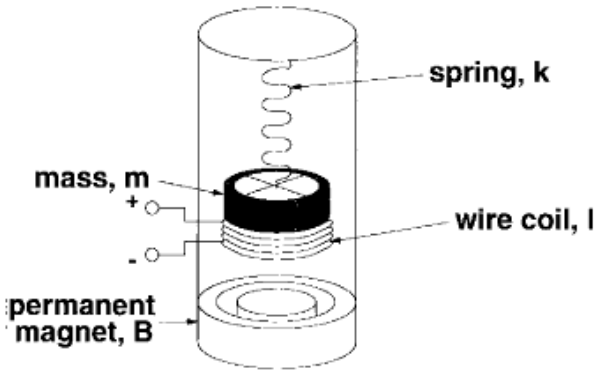

Fig. 2.4: Schematic diagram of an EM energy harvester [13]. The cylinder shell should be attached to the vibration energy source.

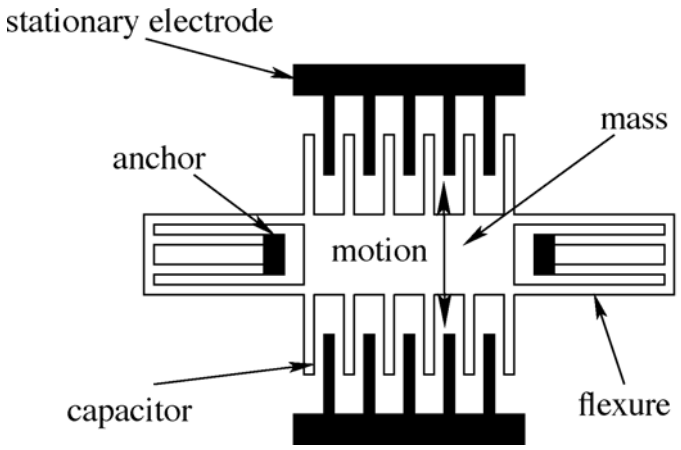

Fig. 2.4. Schematic diagram of an electrostatic energy harvester [43, 69]. The anchor and the stationary electrode are to be fixed with respect to the vibration energy source.

2.2.2 Electrostatic energy harvester

Fig. 2.4 shows the schematic diagram of an electrostatic energy harvester. Before operation, the capacitor (C) between the mass and the stationary electrode has a charge Q, so the energy stored is $\frac{1}{2}\frac{Q^2}{C}$. When the vibration of the energy sources causes movement of the mass, the capacitance (C) between the mass and the stationary electrode varies, leading to a change in voltage. Thus, the mechanical energy can be converted into electrical energy.

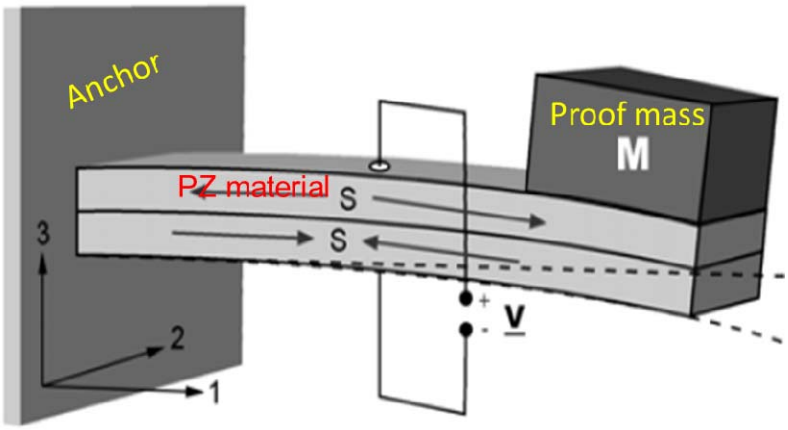

Fig. 2.5: Schematic diagram of a piezoelectric energy harvester [73]. The beam is coated with piezoelectric (PZ) material on both sides; the anchor will be attached to the vibrational source.

The advantage of the electrostatic energy harvester is the easy integration into electronic devices by MEMS[1] process technologies using a process similar to integrated accelerometer manufacturing [43, 70]. The down scaling of the energy harvester, thus obtaining a smaller size, is easier than for the other types of vibration energy harvesters. What's more, the electrostatic energy harvester can be operated at non-resonant mode [71].

The disadvantage of the electrostatic energy harvester is that it needs an external voltage source to give the initial charge Q to the capacitor. It was proposed to solve this by using an electret as a long-lasting charge source [72].

2.2.3 Piezoelectric energy harvester

Fig. 2.5 shows a schematic diagram of a piezoelectric (PZ) energy harvester. A piezoelectric generator is based on the physical phenomenon that, when a piezoelectric material deforms due to motion-induced stress or strain, the polarizations of the electric dipoles are changed. This leads to a voltage difference, thus kinetic energy is converted into electric energy.

The advantage of the PZ energy harvester is that it has high energy density and can be integrated with electronic devices by MEMS technology. The

[1] Micro-electro-mechanical-system

voltage of the output energy harvester can be more than 10 volts, so up-conversion is not necessary [17, 74].

The disadvantage is that the resonant frequency of the PZ energy harvester is higher than that of the ambient vibration sources normally available when the energy harvester is miniaturized. The latter has a typical value below 200 Hz, and the former is well above 1 kHz [54, 74, 75]. Also the PZ material is brittle, so long term mechanic wear out may limit the lifetime of the energy harvester [74].

2.3 Modeling of an integrated EM harvester

All the three aforementioned energy conversion mechanisms have the pros and cons. Taking the requirements of the energy harvester into account (Section 1.2), an on-chip integrated EM harvester by CMOS compatible post processing technology is modelled to study the feasibility of its practical implementation.

In this section, we presented the design of the EM energy harvester and the preliminary simulation results.

2.3.1 Design of the new EM energy harvester

Fig. 2.6 depicts the design of our EM harvester: coils, springs, and a permanent magnet.

The coils are embedded in the CMOS chip, i.e., the coils will be made by metal layers during back-end-of-line processing. So the coils can have 6-8 layers, depending on the choice of (deep-submicrometer) CMOS technology. The standard vias are used to connect the successive layers. As shown in Fig. 2.7, the via-connections and the design of the coil layer are done in such a way that all the coil layers are connected in series.

The mass-spring and the permanent magnet of the EM harvester will be post-processed. Fig. 2.8 shows the design of the spiral or bi-spiral shaped spring, and such designs can provide a low resonant vibration frequency compared to the cantilever beam based spring of an EM generator [64].

The permanent magnet will be attached to the center of the spring, and will act as the mass at the same time. If we choose cobalt platinum (Co-Pt) based

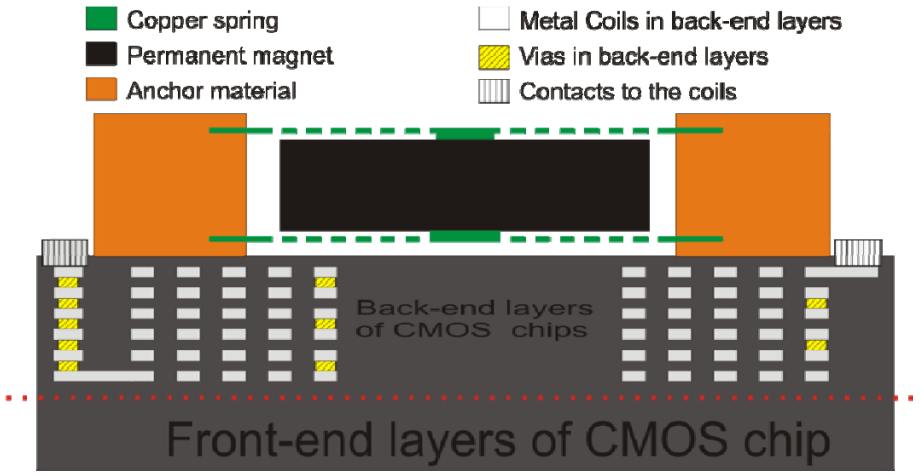

Fig. 2.7. Schematic diagram of the micro scale EM generator (not to scale)

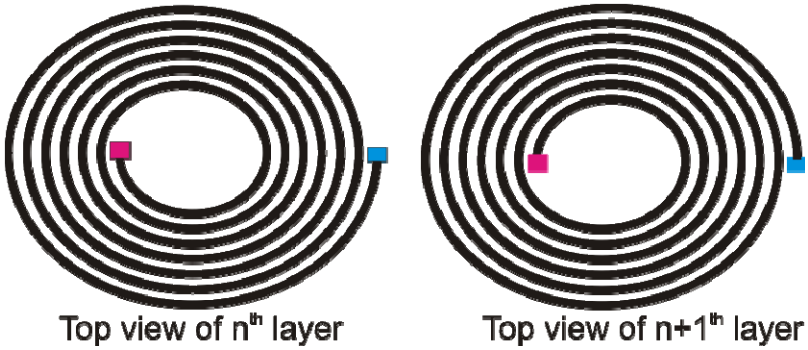

Fig. 2.7. Design (top view of) of the successive coil layers. The spirals are directed clockwise and anti-clockwise, alternatively. Such design makes sure that the EMFs of different layers are superimposed, not canceled.

permanent magnetic material for purpose of monolithic integration [76, 77], then the height of the permanent magnet could not exceed 100 μm.

2.3.2 Numerical Simulations

There are two possible vibration directions of the permanent magnet with respect to the embedded coil: vertical and horizontal, as shown in Fig. 2.9.

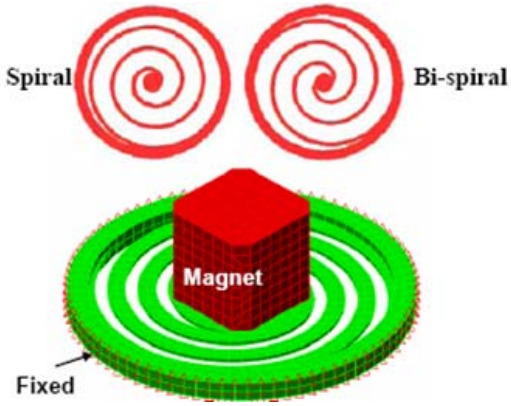

Fig. 2.9. The design of the spring aims for low frequency vibration (adopted from [64]).

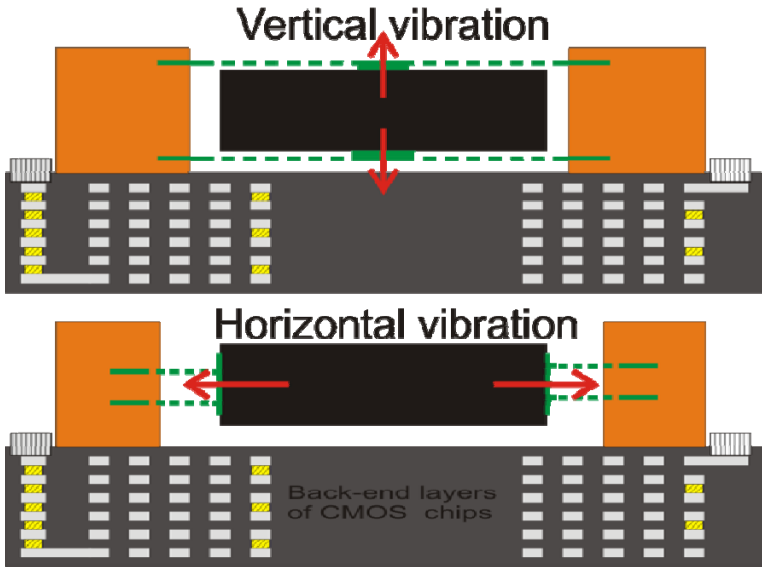

Fig. 2.9. The permanent magnet have two possible vibration directions with respect to the coil layers. The positions and the directions of the coil layers are fixed by CMOS technology.

Numerical simulations have been carried out, by using a COMSOL FEMLAB code [78], to find the amount of power output.

2.3.2.1 Theory of Magnetic field from a Permanent Magnet

From Farady's law, the voltage across the coil ends is proportional to the change of the magnetic flux through the coil. The magnetic flux is induced by

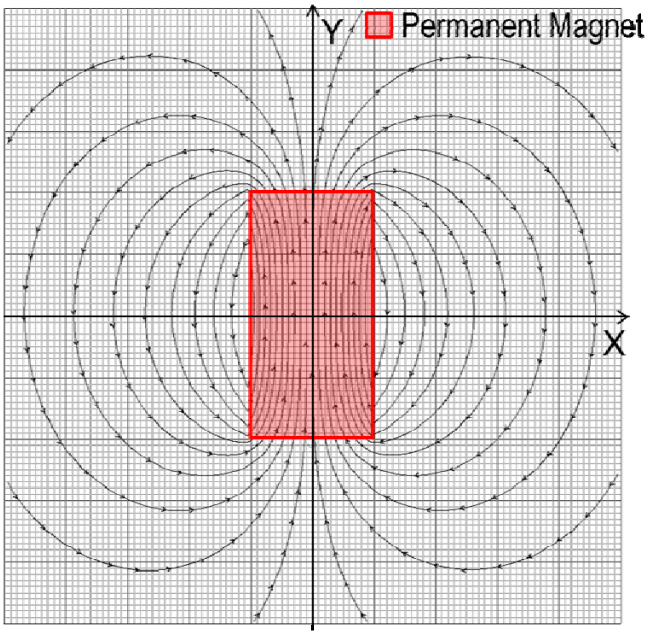

Fig. 2.10. Stray field of a cylindrical permanent magnet simulated by Visimag [79].

the permanent magnet, so the starting point of the COMSOL simulation is the calculation of the magnetic field distribution of a permanent magnet.

Qualitatively, Fig. 2.10 shows a two dimensional magnetic field of a cylindrical permanent magnet.

For infinite element analysis, the permanent magnet is composed of many small pieces, and each of them is called an element. Each element inside the permanent magnet will have its own residual magnetization *M*, volume size dv' and surface area ds'. Each small element will give its own contribution to the magnetic field strength according to Eq. (2.5) - Eq. (2.7). The magnetic field strength at certain position $\vec{x}$ is a superposition of all the small permanent magnet elements.

$$\overrightarrow{B_{(\vec{x})}} = \nabla \times \overrightarrow{A_{(\vec{x})}}$$

$$= \frac{\mu_0}{4\pi} \iiint \overrightarrow{j_{M(\vec{x}')}} \times \frac{\vec{x} - \vec{x}'}{|\vec{x} - \vec{x}'|^3} dv' + \frac{\mu_0}{4\pi} \iint \overrightarrow{j_{M(\vec{x}')}} \times \frac{\vec{x} - \vec{x}'}{|\vec{x} - \vec{x}'|^3} ds' \qquad (2.5)$$

where, $\vec{x'}$ is the coordinate of the contributing permanent magnet element, $\vec{x}$ is the coordinate where we are interested in, dv' is the volume of the contributing permanent magnet element, ds' is the surface area of the contributing permanent magnet element, $\vec{B}$ is the magnetic field strength, $\vec{A}$ is the magnetic vector potential, μ_0 is the vacuum permeability, $\vec{J_M}$ is the magnetic volume current density, $\vec{j_M}$ is the magnetic surface current density.

The magnetic current density $\vec{J_M}$ and $\vec{j_M}$ are given by Eq. (2.6) and Eq. (2.7) respectively:

$$\vec{J_{M(x')}} \equiv \nabla \times \vec{M_{(x')}} \tag{2.6}$$

$$\vec{j_{M(x')}} \equiv \vec{M_{(x')}} \times \vec{n} \tag{2.7}$$

where $\vec{n}$ is the surface normal vector to the surface ds' at position $\vec{x'}$.

These equations can be derived from the Maxwell equations under the quasi static assumptions [80], which are applicable to our case due to the small size of the EM generator and the low vibration frequency.

2.3.2.2 Model

For finite element analysis, a smaller size element will lead to more accurate results. However, the number of the elements is practically limited by computer memory size and computation speed.

An AC/DC module of COMSOL 3.3a has been used to perform the numerical simulations. The mesh of the simulated structure consisted of 39000 elements, i.e., square blocks; the number of degrees of freedom to be solved was 640000. The COMSOL simulates the magnetic field according to Eq. (2.5) - Eq. (2.7), listed in Section 2.3.2.1.

Due to time limitations, simulations are done based on the layout depicted in Fig. 2.11, which is a simplified version of Fig. 2.9. The following text specifies the input parameters for the simulation:

a) The cylindrical permanent magnet has a height of 50 μm, a radius of 50 μm.
b) The permanent magnet has a residual magnetization of 0.5 tesla, and its magnetization direction is along the axis of the coil.

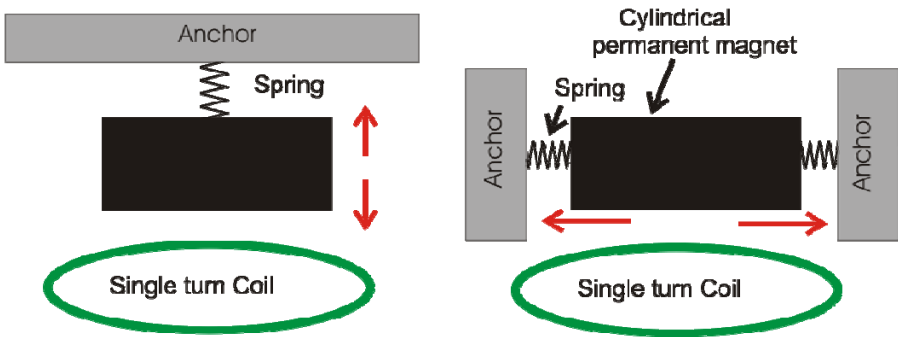

Fig. 2.11. Schematic diagram of the EM-generator model simulated by COMSOL.

c) The resonant vibration frequency of the EM harvester is set to 100 Hz.
d) The vibration amplitude of the EM harvester is set to 5 μm, the space between the coil and the permanent magnet is 10 μm.
e) For this simulation, only a single turn coil with a radius of 60 μm is used. For multiple-turn coils, similar simulations can be carried out.

Input parameters a) and b) for the permanent magnet are based on properties of the CMOS post-processed Co-Pt material [76, 77]. The neodymium-iron-boron (Nd-Fe-B) based permanent magnets offer a higher residual magnetization (1 tesla) [81], but only for a higher process temperature (500 ºC) [82], not allowing CMOS post-processing.

Inputs parameters c) and d) are related to the vibration of the EM harvester, which corresponds to an acceleration amplitude of 0.2g (g is the standard acceleration due to free fall). These parameters are based on the properties of the generally available low-level vibrations (see Section 1.3.2). Here we select a typical value of 100 Hz, which can be achieved by tuning the thickness of the spring and the weight of the permanent magnet.

2.3.2.3 Simulations Results

For the vertical-vibration simulations, as shown on the left in Fig. 2.11, the magnetic flux through the coil and electromotive force (EMF), i.e., the voltage output of the coils, inside the coil versus time are shown in Fig. 2.12 and Fig. 2.13, respectively.

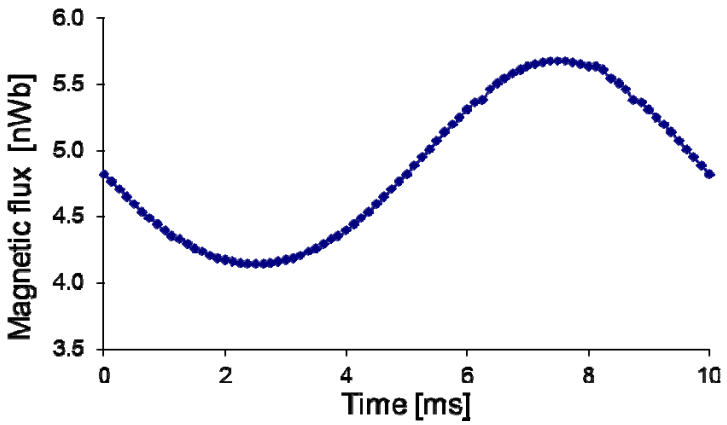

Fig. 2.13. Magnetic flux through a single-turn coil at 100 Hz for vertical vibrations. The simulation results are shown for one period of time, i.e., 10 ms.

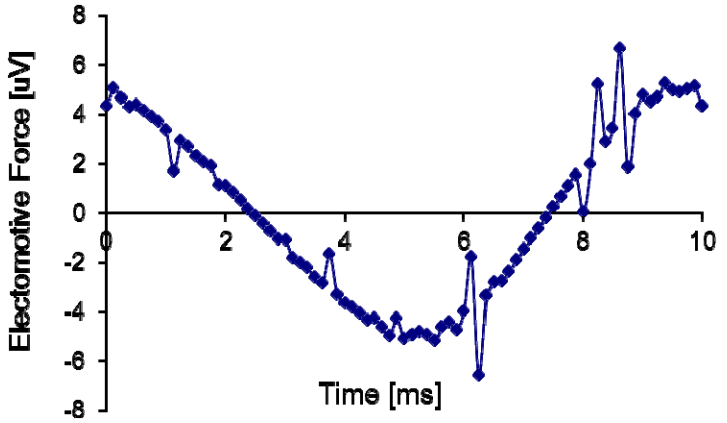

Fig. 2.13. EMF of a single turn coil at 100 Hz (vertical vibrations).The simulation results are shown for one period of time, i.e., 10 ms.

For horizontal vibration as shown on the right side in Fig. 2.11, the magnetic flux through the coil and EMF of the coil versus time are shown in Fig. 2.14 and Fig. 2.15, respectively.

The trend of the horizontal vibrations is not as clear as that of the vertical vibrations. This is due to the large element size in the simulation. More precision could be obtained by a finer computation mesh, however from the results it is clearly established that horizontal movement generates negligible power, so no further study of this mode was pursued.

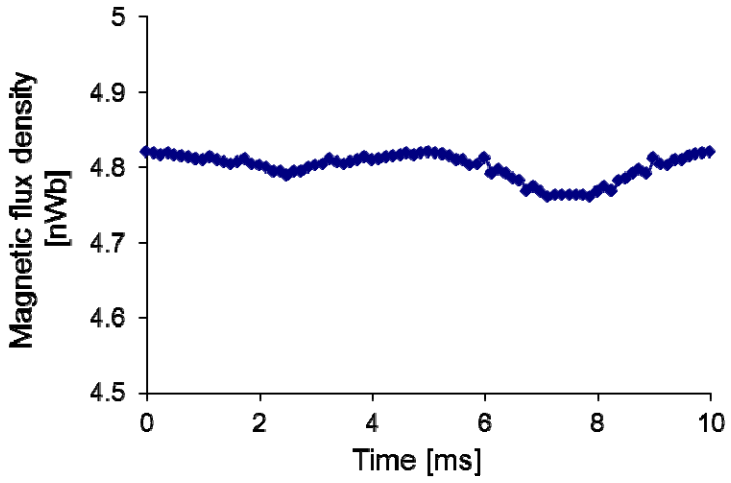

Fig. 2.15. Magnetic flux through a single-turn coil at 100 Hz for horizontal vibrations. The simulation results are shown for one period of time, i.e., 10 ms.

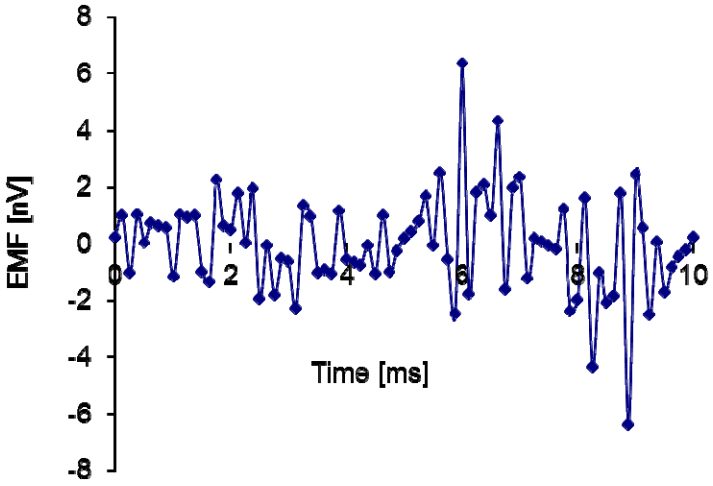

Fig. 2.15. Electromotive force of a single turn coil at 100 Hz for horizontal vibrations. The simulation results are shown for one period of time, i.e., 10 ms.

2.3.2.4 Power estimation and possible improvements

Assuming a 1×4 μm^2 cross section of the coil with the same conductivity as Cu (6×10^7 siemens/m [96]), which is the same material of the metal layers in CMOS chips, the coil resistance R_0 is given by:

$$R_0 = \frac{L}{\sigma S} = \frac{60 \times 2\pi \times 10^{-6}}{6 \times 10^7 \times 4 \times 10^{-12}} = 1.6\ \Omega \qquad (2.8)$$

From Fig. 2.13 , the maximum EMF of the vertical vibrations, which is induced voltage (V) inside the coil, is about 5 μV, so one can obtain the maximum power, that can be extracted, is half of the power dissipated:

$$P_1(\max\_vertical) = V^2/(2R_0) = 7.8\ \text{pW} \tag{2.9}$$

From Fig. 2.15, it is difficult to extract the maximum EMF of the horizontal vibrations because its excursions are difficult to distinguish from noise. The averaged EMF should be orders less than that of the vertical vibrations.

Based on this modeling estimate, we can conclude that a picowatt power output can be obtained from one single-turn coil and the small Co-Pt based magnet. As specified in Section 1.2, we need to increase the power output to the microwatt range. Because the PM magnet's size is limited due to the fabrication technology [76, 77], and because of the size limitations for smart dust, we consider two other possible ways to improve the power output.

First, for each small EM harvester, we increase the number of coil turns to N_1, the improvement of the power output is proportional to the number of coil turns:

$$P = \frac{V^2}{2R} = \frac{1}{2N_1R_0}\left(\frac{N_1 d\phi}{dt}\right)^2 = N_1 P_0 \tag{2.10}$$

where we assume, R_0 is the resistance of one single-turn coil, P_0 is the power extracted from the single-turn coil.

Second, like batteries connected in series, we can connect a lot of small EM harvesters in series. The improvement of the power output is proportional to the number of the EM harvesters connected (if the EM harvesters vibrate in phase).

If we use N_2 to denote the number of EM harvesters connected, then the power output will be given by Eq. (2.11).

$$P = N_1 N_2 P_0 \tag{2.11}$$

As to the value of N_1, it can have a decent value of 20~30. Because in our design the coils of the EM harvester are a part of the metal layers of the CMOS chip, the number of coils layers should be the same as that of the metal layers. In each layer, the number of coils is limited by the size of the small permanent magnet. Assume a typical 6-metal layers CMOS chip, and each layer having 4~5 turns of the coil, the value of 20~30 for N_1 is realistic.

As to the value of N_2, it is limited by the total size of the smart dust. For a typical smart dust size of 1 cm^3, the number of the allowed small EM harvesters is given by Eq. (2.12).

$$N_2 = \frac{1\ cm \times 1 cm}{123\ \mu m \times 123\ \mu m} = 6400 \tag{2.12}$$

Note: assuming the space between the adjacent small EM harvester to be 5 μm, the diameter of the small permanent magnet is 120 μm and the total size of the magnet matrix size of 1 cm^2 .

So according to Eq. (2.11), the total possible power can be:

$$P = N_1 N_2 P_0 = 30 \times 6400 \times 7.8\ pW \approx 1.5\ \mu W \tag{2.13}$$

So the numerical simulation shows that the vertical vibrations of the permanent magnet offer higher power output, and energy scavenging in the microwatt range is possible by connecting a matrix of small energy harvesters in series.

2.3.3 Discussion

Ching, *et al.* reported a power output of 830 μW [64], which is the highest power output of a micromechanical EM harvester according to my knowledge. Compared to that, the power output from our model is very low.

There are two reasons: the permanent magnet used by Ching *et al*. is Nd-Fe based off-the-shell product which has a higher magnetic field; and the vibration amplitude of their EM harvester is set to 200 μm, which is 40 times larger than that used in our simulations.

According to Eq. (2.2) - Eq. (2.4), the power output is proportional to the square of the vibration amplitude. If we take this into account, then our simulation result is comparable to Ching's experimental value.

2.4 Frequency match challenge

As shown in Section 2.1, the vibration based energy harvester harnesses the harmonic oscillation that the vibrating energy source stimulates. In turn, ensuring proper oscillatory motion plays a major role in the resonant converter design.

Due to the omnipresence of the vibration energy source, the vibration-based energy harvester attracts attention of the researches for already many years. Within the last several years, researchers of vibration-based power generation acknowledged a huge challenge: the frequency match.

First, the resonant frequency of the vibration-based energy scavenger is often larger than 1 kHz [43, 75] when one tries to miniaturize the scavenger down to cubic centimeter size. Most of the available ambient vibration energy sources have a frequency below 200 Hz [16]. So these two frequencies are difficult to match. As can be seen from Eq. (2.2), the output power will decrease exponentially with increasing of this mismatch.

Second, the bandwidth of the resonance peak of the miniaturized energy harvester is less than 5 Hz [43, 75, 83]. The smart dust concept does not allow for large arrays of harvesters with their own resonant frequency. So such a narrow bandwidth will limit the flexibility of such energy harvester, i.e., for every application and for every ambient vibration source, a specific energy harvester has to be designed for obtaining a good match.

Although there are efforts in addressing the frequency match problem (unfortunately still leading to a reducing power output) [84-88], there is no practical way to overcome this fundamental challenge.

2.5 Conclusions

In this chapter, the vibration-based energy harvester has been discussed. An EM energy harvester suitable for monolithic above-CMOS-chip integration is proposed. The numerical simulation results show that, within the most practical device dimensions (1 cm^3), the power output in the micro-watt range is feasible and the results are comparable to those found in literature.

However, the practical realization of the proposed design has not been pursued due to the following reasons:

1. The MESA+ Nanolab offers no multilevel metallization capabilities, nor thick-film magnetic layer depositions. Experimental work would therefore depend on the cooperation with two external parties: one for the metallization, another for the magnet.
2. The frequency-match problem mentioned in Section 2.4 convinced us that, even if finally our EM harvester was successful, the operating

window would be very small. Thus the application would be seriously limited and not suitable for mass production.

Considering the aforementioned practical difficulties and under the shadow of the fundamental limitation of the vibration-based harvester, we decided to focus on thin-film solar cell approaches for energy harvesting as described in the following chapters of this thesis.

Chapter 3. Solar cells on top of CMOS chips as energy harvester

In this chapter, the idea of monolithic integration of a solar cell on top of deep-submicron CMOS microchips as an energy harvester for "smart dust" is presented. First, a brief introduction to solar cells will be given, followed by the selection of solar cell technology for the integration. Further the results of the deposition of passivation layers, essential for protecting the CMOS chip, will be presented.

3.1 Choice of the technology

As already discussed in Section 1.4, solar cell is a competitive candidate as an energy harvester. In this section, we detailed the reasons for monolithical integration thin-film amorphous-silicon (a-Si) solar cells and copper indium gallium (di)selenide (CIGS) solar cells on top of CMOS chips without changing either the CMOS process or the conventional solar cell process flow.

3.1.1 Monolithic Integration

There are two approaches to realize a solar-cell-based energy harvester: hybrid-assembled and monolithic integration. Hybrid assembly is off-the-shelf, allows rapid prototyping, and offers the freedom of using different sizes for the energy generating and the energy consuming parts.

On the other hand, monolithically integrated devices bear the promise of a smaller overall size, and reduced manufacturing cost per system. Because the processes such as flip-chip/ball grid arrays, yields are sometimes much lower than 100%, in particular for off-mainstream products, so the monolithic integration may also offer a higher yield. The existing silicon on bulk-silicon [89] or on SOI [90] wafer can be used as the photo conversion medium. Our approach takes a different route, along the "Above-IC" processing philosophy (see e.g. [19]). By creating a photovoltaic cell above an existing IC, the transistor and interconnect density are uncompromised and freedom of choice appears for the solar cell technology. We will discuss the particular choice of the solar cell technology in the next section 3.1.2.

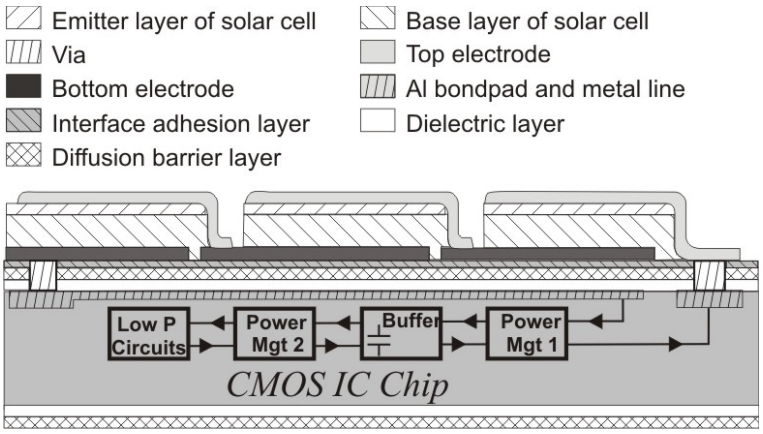

Fig. 3.1. Envisaged autonomous microchip comprising of a PV cell for energy collection, power management circuits, integrated energy storage (e.g. high-density capacitor or solid-state battery) and low-power circuits. The PV cell can be realized on the chip's front or back side.

The conversion efficiency is higher than that of hybrid assembly due to the minimized wiring. Less area is lost for daisy-chain connections, as standard lithography can be used on wafer scale production, contrary to large scale photovoltaic (PV) production [91]. Finally, smaller cell sizes typically lead to a 3~5% [22] efficiency boost.

Fig. 3.1 shows the monolithic integration of a solar cell on a chip by "above-IC" CMOS post-processing. The daisy-chained solar cells convert light into electricity; the generated power is supplied to the underneath CMOS chips by the vias and the aluminum leads. The chip electronics, besides the low power functional circuits, include energy storage and management modules (common to all energy-harvesting systems). Temporary energy storage can be provided using an integrated high-density capacitor or solid-state battery. One possible attractive approach (not pursued in this work) is to employ the upper interconnect layers of the CMOS chip to this purpose. Between the CMOS chips and the solar cells, an intermediate film (or stack of films) is required to serve three purposes: for electrical insulation, to create a diffusion barrier against impurity contamination and for a better adhesion.

3.1.2 Solar cells selected as energy harvesters

In this section, we show that a thin-film amorphous-silicon solar cell and copper indium gallium (di)selenide (CIGS) solar cells are good candidates to be manufactured directly on a CMOS chip.

3.1.2.1 Brief history

Solar cells or photovoltaic (PV) cells generate electricity when illuminated by sunlight or artificial light. The discovery of the photovoltaic effect is normally ascribed to Becquerel in 1839 [92], and selenium based solar cell, the first direct conversion of the energy of light into electricity energy, was invented by German physicist, Fritts, in 1883 [92]. In 1954, Chapin *et al.*, from Bell laboratories, fabricated the first modern silicon solar cell with 6% efficiency [93]. Due to the persistent research efforts worldwide, mainly in USA, Europe and Japan, more than 10 solar cell technologies emerge and the highest efficiency reaches to 27.6% and 32.0% for single-junction and multi-junction solar cells, respectively [22]. Fig. 3.2 shows the solar cell efficiency evolvement in the last century for different technologies [94]. Due to the awareness of the global warming, carbon-free energy becomes more and more impotant in the past 10 years. As the world's major renewable green energy source, the solar cell has huge development in the past 10~20 years.

However, it is more or less generally accepted that among all the solar cell technologies, only those using thin films are likely to be able to reach the very low costs and can meet the long term demands of the electricity and energy market [95]. Nowadays, there are three main thin film technologies that are successfully commercialized: a-Si, CdTe and CIGS solar cells. In 2011, the record efficiencies are 10.1%, 16.7%, 20.3% for a-Si, CdTe and CIGS solar cells, respectively. Fig. 3.2 also shows the evolvement of these three types of thin film solar cells by the end of last century [94].

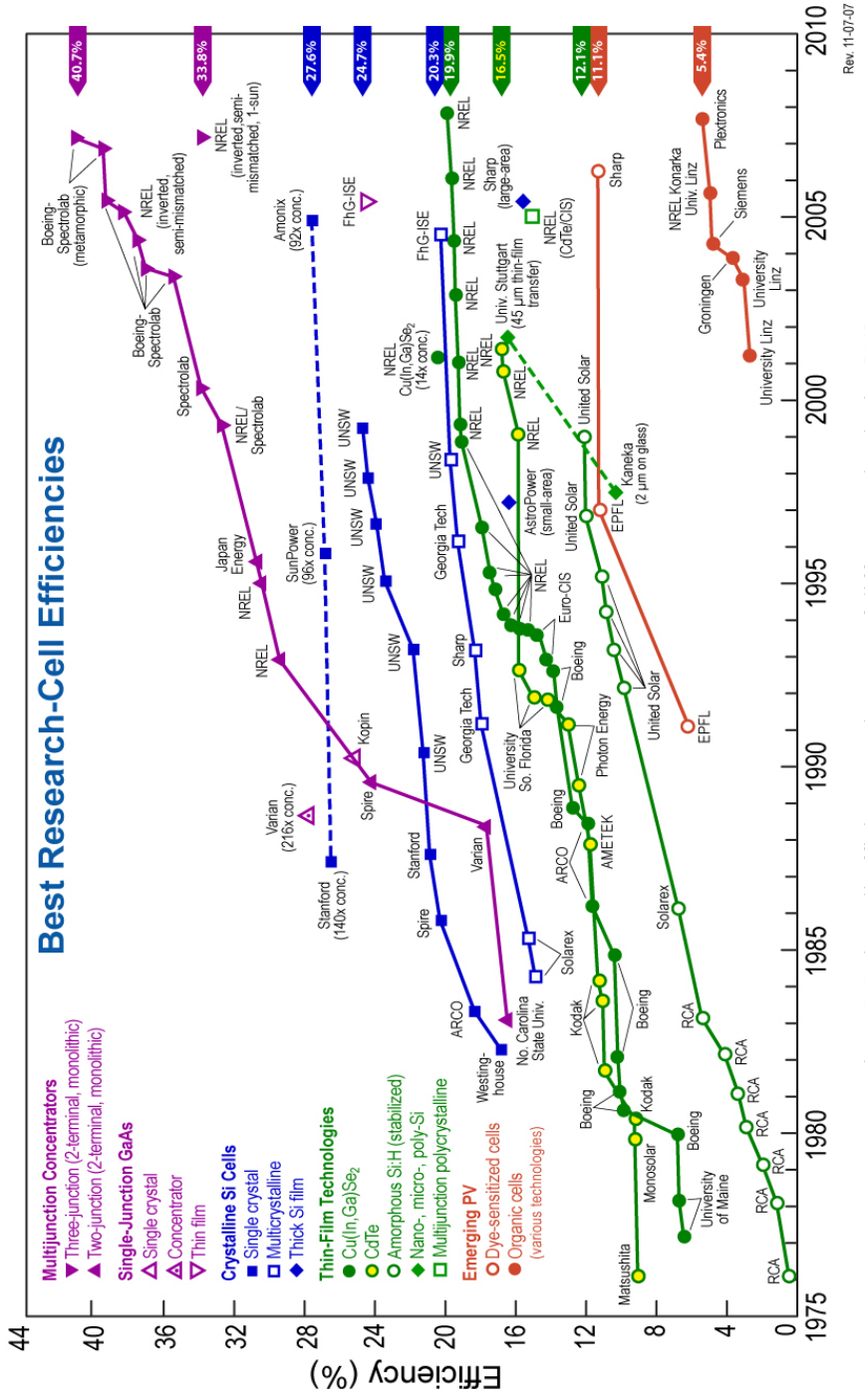

Fig. 3.2. Solar cell efficiency evolvement of different technologies [94].

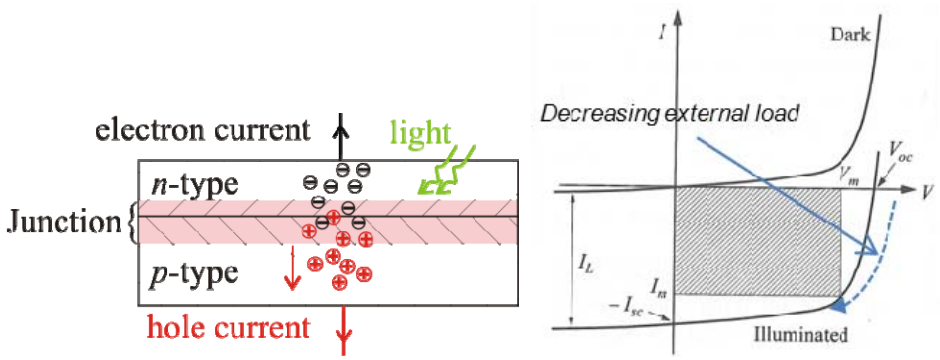

Fig. 3.3. Simplified physical model of a solar cell. Left, solar cell as a p-n diode to convert light to electricity; right, typical p-n diode I-V characteristics of a solar cell with decreasing external load under dark and illumination.

3.1.2.2 Basic theory

Intrinsically, most of the solar cells can be viewed as a p-n junction diode. The basic principle of the solar cells is fully explored in many books [21, 96-99], and here only a concise and qualitative description is given.

Fig. 3.3 shows the simplified physical model of a solar cell and the I-V characteristics of the solar cell in dark and under illumination with light. On the left-hand side, the electron and hole pairs (EHPs) are generated after the photon is absorbed by the solar cell material, which is a semiconductor p-n junction for most of the PV technologies. Before electron and hole recombine, the internal electric field at the p-n junction of the solar cell has to separate them, driving the electrons to the n-region and holes to the p-region.

In the absence of external connections, the drift current is exactly offset by a reverse diffusion current caused by the carrier concentration gradient. This leads to the open-circuit voltage (V_{oc}), being established across the contacts to the two regions. At this point, no current flows through the load.

With an external load across the external contacts to the device, the photo generated excess carriers will flow through the load, thus giving a PV current. When the device is fully short-circuited, the short circuit current (I_{sc}) flows though the load, and no net voltage appears across it.

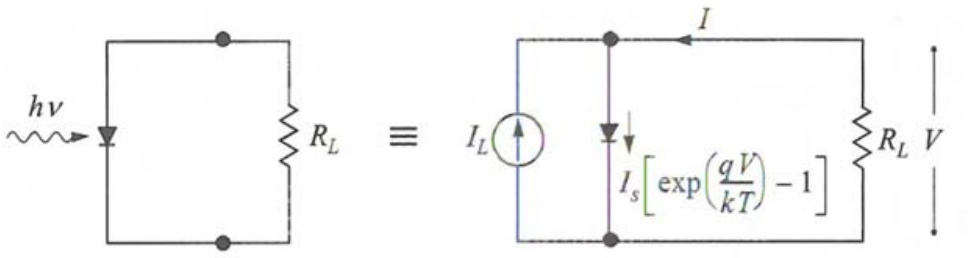

Fig. 3.4. Simplified electrical circuit model of a solar cell under illumination [96].

The maximum power, P_{max}, generated by the device , is defined by the following equation:

$$P_{max} = (VI)_{max} = V_m I_m \tag{3.1}$$

Solar cells should operate at the maximum power point, where the system can operate most efficiently. This is indicated as the shadowed region indicated on the right in Fig. 3.3.

The fill factor (*FF*) measures the sharpness of the I-V curve and is defined:

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} \tag{3.2}$$

And the solar cell efficiency (η) is the ratio of the maximum power output to the incident power of the illuminating light, P_{solar} :

$$\eta = \frac{V_m I_m}{P_{solar}} \tag{3.3}$$

Fig. 3.4 shows a simplified equivalent electric circuit of a solar cell under illumination. From this model, the total current under illumination is a sum of the dark current and the photo generated current:

$$I = I_s\left(e^{qV/kT} - 1\right) - I_L \tag{3.4}$$

where I_s is the saturation current, and its value can be obtained be from Eq. (3.5), V is the bias voltage of the solar cell, q is the unit electric charge, k is the Boltzmann constant, T is the operating temperature of the solar cell, I_L is the photo generated current, and roughly equals to short circuit current, I_{sc} .

$$I_s = I_{sc}\left(e^{qV_{oc}/kT} - 1\right)^{-1} \approx I_{sc} e^{-qV_{oc}/kT} \tag{3.5}$$

In practical, Eq. (3.6) predicts *I-V* characteristics of a solar cell [100].

$$I = I_s\left(e^{q(V - IR_s)/nkT} - 1\right) - I_L \tag{3.6}$$

Table 3.1: Solar cell efficiency at outdoor (AM 1.5) and indoor light illumination conditions. Data are from [23, 24, 105]. The indoor light is the reduced-intensity AM1.5 spectrum; the c-Si, a-Si solar cells are the commercial products, the others are laboratory samples (see references [23, 24, 105]).

	Bulk solar cells		Thin-film solar cells			
Light intensity	c-Si	GaAs	Photo-chemical	CdTe	a-Si	CIGS
Outdoor AM1.5	12.5%	12.4%	4.0%	4.7%	7.5%	12.9%
Indoor 10 W/m^2 *	3.2%	8.7%	4.7%	3.7%	6.7%	7.7%

where n is the ideality factor for the solar cell, R_S is the series resistance.

3.1.2.3 Solar cell technologies for indoor light

For a broad range of applications, solar cell energy harvesters should also be used at indoor light conditions. However, the indoor light spectrum is quite different from the solar cell spectrum at surface of the Earth (AM 1.5 illumination) [101]. A well-performed solar cell under AM 1.5 illumination (100 mW/cm^2) may have poor performance under indoor light spectrum and weak light conditions (0.1~10 mW/cm^2) because how photons are absorbed by a solar cell depends on the photon energy and the band gap of the semiconductor material of that solar cell. For example, employing monocrystalline silicon (c-Si) solar cells for indoor energy harvesting, researchers found that the indoor efficiency of c-Si is only 10~40% percent of the outdoor efficiency, due to a mismatch of the c-silicon band gap with the indoor fluorescent light spectrum [24, 102-104]. So given our ambition to make ubiquitous energy harvesters, the selection of the thin-film solar cell technology is critical.

From Table 3.1, one can see that particularly c-Si solar cells have relatively poor indoor efficiency. Other technologies, such as a-Si or CIGS solar cells can maintain an efficiency around 7% under indoor light illumination.

Other considerations further narrow down the choice of solar cells integrated on CMOS chips. We discarded CdTe-based cells in view of the environmental concerns with cadmium, which might hamper industrialization (the replacement of lead in solder has been a painstaking process in the

electronics industry [106]). Photo-chemical dye solar cells, as well as the currently known polymer solar cells, have stability concerns over the micro-system's envisaged lifetime [107, 108].

Thus we ended up with a-Si and CIGS solar cells as the most attractive candidates for the monolithic integration. CIGS-based cells have the highest efficiency among the existing (thin-film, mono-junction) types, be it at relatively high process temperatures [109]. Also a-Si solar cells perform very well at indoor-light illumination conditions. The amorphous silicon approach can be expanded to create tandem cells for higher efficiency and higher output voltage. For both CIGS and a-Si technologies, the production equipment is suitable for low-cost monolithic integration on CMOS.

3.1.3 CMOS chips selected for monolithic integration

In order to investigate the generic applicability of our monolithic integration approach, we will integrate both the a-Si and CIGS solar cells on CMOS chips of different technologies and with different functionality. Table 3.2 shows the technological specifications of the chosen CMOS chips.

Timepix chip [110] is a mixed-signal CMOS chip processed by 6-metal 0.25 μm technology utilizing shallow trench isolation (STI) and aluminum interconnects. Its active part consists of 256 columns of 256 pixels, and each pixel contains 550 transistors. It is designed to be ball-grid-connected to a semiconductor sensor layer (e.g. CdTe) and also employed in other two-dimensional radiation imaging detectors [111, 112].

The Ringo CMOS chip is a 6-metal 0.18 μm CMOS with Al interconnect, where saw-line process control modules (PCMs) with ring oscillators were characterized.

The Cu-PCM is a 0.13-μm technology CMOS chip with copper interconnects. We used PCMs processed up to the first-metal. Individual MOS capacitors and transistors are available for on-wafer probing in the PCM modules.

The bond pad regions are located at the edge of Timepix chip, those of Ringo chip are located at the dicing-lane. For Cu-PCM, the bond pads are distributed all around the chip close to the single devices, i.e., there is no

Table 3.2: Technological specifications for CMOS chips used in light harvesting integration experiments. Data are from [23, 24, 105]. The indoor light is the reduced-intensity AM1.5 spectrum; the c-Si, a-Si solar cells are the commercial products, the others are laboratory samples (see references [23, 24, 105]).

Abbreviation	Technology (μm)	Metal levels	Interconnect	source	Comments
	Bulk solar cells			Thin-film solar cells	
Timepix	0.25	6	Al	CERN	Functional chip
Light intensity	c-Si	GaAs	Photo-chemical	CdTe	a-Si / CIGS
Ringo	0.18	6	Cu	NXP Nijmegen	Integrated circuit
Outdoor AM1.5	12.5%	12.4%	4.0%	4.7%	7.5% / 12.9%
Cu-PCM	0.13	6	Al	NXP IMEC	Individual MOS capacitors and transistors
Indoor 10 W/m^2 *	3.2%	8.7%	4.7%	3.7%	6.7% / 7.7%
Other PCM	2	1	Al	MESA+ Nanolab	Specified function

separate region for bond pads. This complicates characterization of the devices after a solar cell is deposited on top, as discussed later on.

During our experiment, other PCM chips fabricated at our university were also used. This chips are fabricated in MESA+ NanoLab [113], which is a class 100 cleanroom. The starting materials were p-type <100> 4 inch silicon wafers with 5-10 ohm· 393939393939393939393939393939

The possible damages were listed in Section 1.2.4, we use these three different CMOS chips to monitor the possible influence of the post-process: Different technology generations CMOS chips can give generic information about the integration compatibility on three different levels: single MOS capacitor, MOSFET, single circuits (ring oscillator), to a completed CMOS chips. If there is a metal ion contamination, then flat band voltage of the MOS capacitor will change, if there is plasma charging on the gate oxide, then the gate leakage current of the MOSFET will change. If the process temperature is too high, then the performance of the Timepix will change. If there is a mechanical stress, then solar cells' front-side integration and backside integration will influence CMOS chips differently.

3.2 Passivation layers for post-processing

As mentioned in Section 1.2, a passivation layer is needed to prevent possible mechanical and/or electrical damage to the CMOS chips by the post-processing steps before the solar cell integration [19].

Here we present the passivation layer deposition and the electrical measurements of the chip performance before and after post-processing, to evaluate the influence of the passivation step.

Plasma enhanced chemical vapor deposition (PECVD) technique were used to deposit the passivation layers. PECVD of 500 nm SiO_2 and 300 nm Si_3N_4 are for the aforementioned purpose. In order to improve the adhesion between the solar cell and the CMOS chips, PECVD of 250 nm SiO_2, 300 nm Si_3N_4 and 250 nm SiO_2 stacks may also utilized. After the passivation, the IC chip underwent thermal annealing for 30 minutes at 400 °C in N_2 atmosphere for outgassing the abundant hydrogen incorporated into the passivation layer.

For Cu-PCM chips, in order to retest the performance of the CMOS chip after the solar cell deposition, the passivation layers needs to be removed by wet-etching in BHF. In order to protect Cu bond pads and the low-k dielectric material of the Cu-PCM from BHF, a 100 nm TiW layer is additionally inserted before the deposition of the passivation layers. After the removal of the passivation layer, the TiW layer was etched off by H_2O_2 solution without attacking the Cu bond pads [114].

3.2.1 Deposition of Passivation layers

The PECVD technique offers a low-temperature process and a reasonable deposition rate, so we use it to deposit the passivation layers: the SiO_2 was deposited at 300 °C with an RF frequency of 187.5 kHz by Oxford 80 system [115], and a process pressure of 650 mTorr. The Si_3N_4 was deposited at the same temperature with an RF frequency of 13.6 MHz and 1000 mTorr process pressure. A 500 nm SiO_2 was deposited during 15 minutes, and 300 nm Si_3N_4 in 15 minutes also. The layer thicknesses were measured by ellipsometer.

The TiW layer was deposited (sputtering) by an Oxford 400 system [115] with a corresponding Ti/W target of 20/80 at%. The magnetron sputtering was done in Ar ambient at 10 mTorr. A 100 nm thick TiW layer was deposited during 130 seconds. The layer thickness was measured by a Dektak surface profiler.

3.2.2 Electrical characterization

Referring to the possible influence of the post-process to the CMOS chip listed in Section 1.2.4 [19], the influence of the passivation layer deposition described in Section 3.2.1 on the CMOS chip may occur due to the high process temperature, the mechanical stress of the added layer, and the hydrogen coming from the PECVD Si_3N_4 layer.

To clarify this, capacitance-voltage (*C-V*) curves of the MOS capacitor and current-voltage (*I-V)* curves of the MOS transistor have been obtained by a Keithley 4200 SCS system before and after the passivation layer stack realization.

Also to investigate the effect of the high temperature, simple experiments of Timepix chips annealing without any passivation layer in Ar ambient was carried out. The electrical characterizations have been done before and after this annealing experiment.

The results are presented and compared below.

3.2.2.1 CV characterization of MOS capacitors on Cu-PCM chips

The MOS capacitor has an area of 144×10^{-8} cm^2 and the oxide thickness is around 2.2 nm. All the capacitance measurements were done at a frequency of 1 MHz.

The CV curves of a MOS capacitor at different stages of processing are shown in Fig. 3.5. The extracted oxide capacitance, C_i, the depletion capacitance, C_D, and the flat band voltage, $V_{FB,}$ are listed in Table 3.3. The oxide charge of the MOS capacitor is calculated from [96, 116] and is shown in the last column of Table 1.1.

The flat band voltage shifts to the left after the post-processing indicates an increase of positive oxide charge ΔQ. The corresponding oxide charge density change is in the order of $10^{11}/cm^2$.

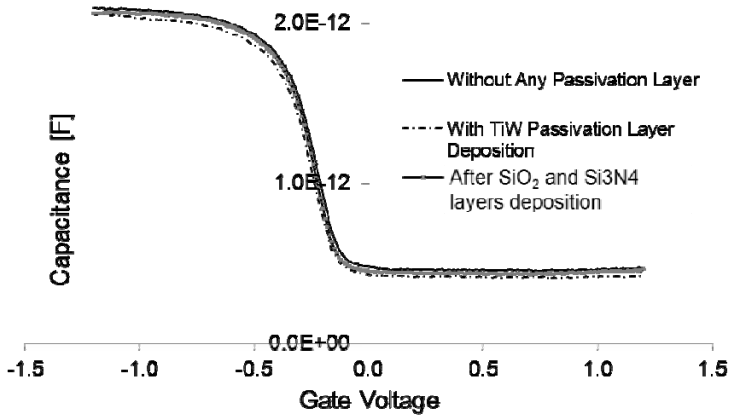

Fig. 3.5. Typical CV curves of a MOS capacitor before and after the passivation layer stack deposition. First, 100 nm thickness of TiW is deposited, then 500 nm SiO_2 and 300 nm Si_3N_4 were added.

Table 3.4. Typical MOS capacitor parameters before and after post-processing .

Chip status	C_i (pF)	C_{min} (pF)	C_D (pF)	V_{FB} (mV)	ΔQ (cm^{-2})
No passivation	2.1	0.47	0.6	-280	\
TiW	2.06	0.42	0.52	-350	3.6×1011
SiO_2/Si_3N_4	2.06	0.45	0.58	-310	2.6×1011

3.2.2.2 Characterization of MOS Transistors on Cu-PCM chips

The MOS transistors on Cu-PCM chip have a gate length of 130 nm. For all measurements of the transistors, the source and the body were connected, i.e., $V_{BS} = 0$ V. The typical drain current against gate voltage (I_D-V_{GS}) curve before and after the passivation layer deposition is shown in Fig. 3.6. The I_D-V_{GS} curves overlap with each other before and after post-processing.

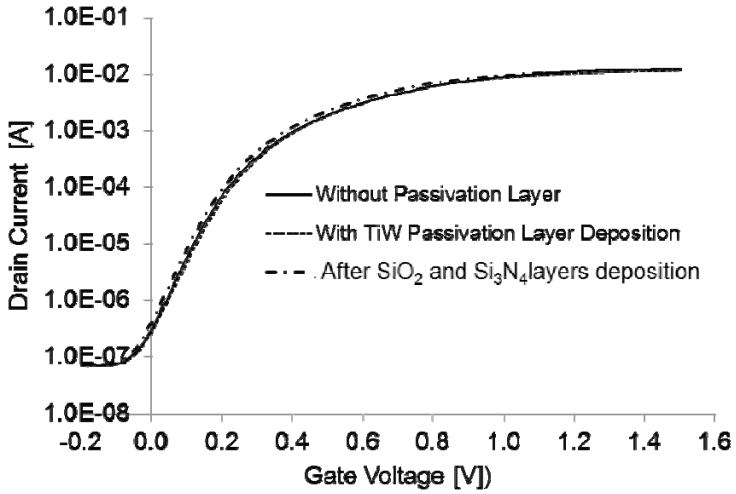

Fig. 3.6. Drain current against gate voltage before and after the passivation layer deposition. First, 100 nm of TiW is deposited, then 500 nm SiO_2 and 300 nm Si_3N_4 were added. Three curves overlap with each other, and show no visible difference.

Table 3.5. Typical MOS transistor parameters before and after post-processing

	No passivation	TiW passivation	SiO_2/Si_3N_4 passivation
I_{Leak}(μA)	13.8±0.5	13.9±0.5	13.9±0.4
I_{On} (mA)	9.0±0.4	8.9±0.3	9.5±0.4
V_{th}(mV)	-88.8±11.9	-87.5±3.3	-94.1±3.1
S (mV/decade)	80.4±1.7	79.6±1.0	77.7±0.7

The gate leakage current, I_{Leak}, the drain saturation current, I_{On}, the threshold voltage, V_{th}, and the subthreshold swing, S, are averaged over 8 transistors. The results are shown in Table 3.4. The change for all the parameter is less than 5%, and for the most important parameter, the threshold voltage, a 1.2 and 6.7 mV shift occurred after TiW and SiO_2/Si_3N_4 layer deposition, respectively.

3.2.2.3 Electrical characterization of Timepix chips

The Pixelman software [117] and an automated probe station were employed for functional testing of the Timepix chips at the Nikhef Institute in Amsterdam (NL). The program tests the functionality of analog CMOS circuitry arranged in 256 columns of 256 pixels. It should be noted that the

Table 3.7. Digital and analog test results of the Timepix chip before and after passivation layer deposition on the chip's front side. The passivation layer composed of 500 nm PECVD SiO_2 first and then 300 nm PECVD Si_3N_4.

	Digital Testing		Analog Testing	
	Bad columns (out of 256)	Bad pixels (out of 65536)	Bad columns (out of 256)	Bad pixels (out of 65536)
Before	20	5120	20	5122
After	20	5119	20	5123

Table 3.7.Digital and analog test results of the Timepix chip before and after pure Ar ambient annealing.

	Digital Testing		Analog Testing	
	Bad columns (out of 256)	Bad pixels (out of 65536)	Bad columns (out of 256)	Bad pixels (out of 65536)
Before	4	1023	4	1015
After	4	1033	4	1015

post-processed chips were of a lower-quality category than those normally used. A fraction of the pixels and columns therefore malfunctions before the solar cell integration as seen in the second row of Table 3.5.

From Table 3.5, it can be inferred that the numbers of bad columns for both the digital and analog test remain the same, before and after the passivation layer deposition. So the Timepix chip is not influenced by the passivation deposition on the front side.

From Table 3.6, the numbers of bad columns for both the digital and analog test remain the same, before and after a pure 30 minutes annealing at 400 degrees at Ar ambient. So the Timepix chip is not influenced by the thermal budget of the deposition.

3.2.3 Conclusions

The passivation layer stack deposition hardly influences the performance of the CMOS chips. There are small changes of the transistor performance, but they are random and probably insignificant. All the changes of the transistor parameters are less than 5%. The functionality of Timepix chips (both analog and digital) was found unaffected by passivation layer deposition. This offers the possibility of further post-processing steps, i.e., deposition of a variety of other functional layers towards solar cell integration.

3.3 Summary

In this chapter we first gave an introduction to solar cells. After that we showed that integration of a-Si solar cells or CIGS solar cells are suitable candidates for above-CMOS integration solar cells energy harvesters. In the rest of the chapter, we present that passivation layers deposition on CMOS chips, which are the initial post-processing steps of solar cells integration, will not influence the performance of the CMOS chip. In the rest of this thesis, we will further present the results of a-Si solar cells integrations (Chapter 4) and the CIGS solar cells integrations (Chapter 5).

Chapter 4. a-Si solar cell integration

In section 3.1, we concluded that monolithic integration of solar cells on top of the CMOS chip is a feasible and competitive approach to energy harvesting for ubiquitous computing. In this chapter, the a-Si solar cell monolithic integration is presented.

4.1 a-Si solar cell introduction

4.1.1 Brief history

In 1965, Sterling and Swann found that Si, SiO_2 and Si_3N_4 layers can be deposited by chemical vapor deposition (CVD) promoted by radio frequency discharge of silane-containing gases [118]. In 1969, Chittick, Alexander and Sterling reported the amorphous silicon (a-Si) thin film deposited by this technique [119]. Between 1975 and 1976, Spear and Le Comber discovered that a-Si thin films can be n- or p-type doped by adding PH_3 or B_2H_6 to silane [120, 121]. In 1976, Carlson and Wronski from RCA laboratories, Princeton, demonstrated the first a-Si solar cell with an efficiency above 2% [122]. Also in the same period, researchers realized that an a-Si thin film was in fact an alloy of silicon and hydrogen, so it was called hydrogenated amorphous silicon (a-Si:H) [91]. The aforementioned events basically marked the beginning of the exploration of a-Si thin films for solar cell technology.

After almost 40 years of intensive research, the a-Si:H based solar cell technology has been evolved from pure single- into double- [123, 124] and triple-junction cells [125, 126]. The thin film material evolved from purely a-Si into hydrogenated microcrystalline (μ-Si:H) layer [127] and alloy of hydrogenated silicon and germanium ($Si_{1-x}Ge_x$:H). Also the technology nowadays is already mature enough for large-scale production [99, 128]. Until 2011, record stabilized efficiencies were confirmed as following [22]: 10.1±0.3% for a-Si:H, 10.1±0.1% for μc-Si:H. Higher efficiency was reported for double junction cells (11.9±0.8% for a-Si/μc-Si) and for triple junction cells (12.5±0.7% for a-Si/nc-Si-nc-Si and 12.3% for a-Si/a-SiGe/a-SiGe).

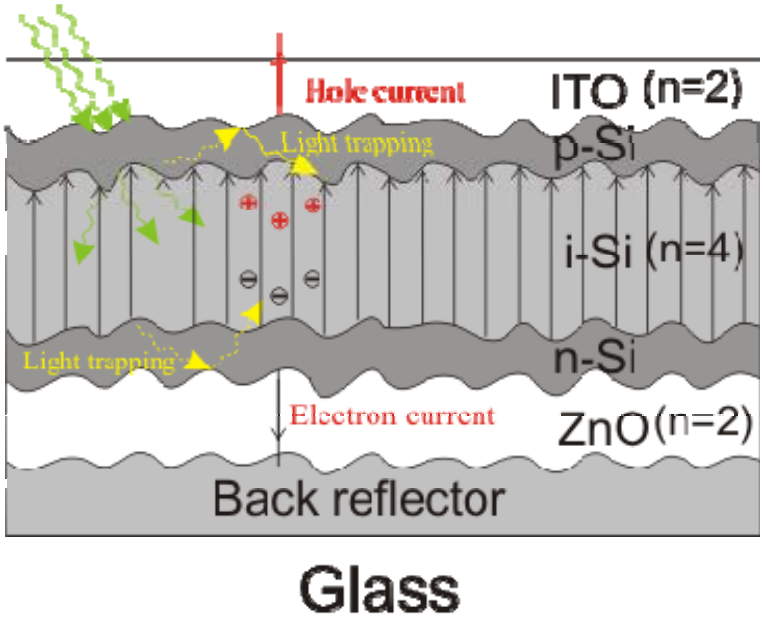

Fig. 4.1. Schematic sketch of an ideal p-i-n a-Si:H solar cell. The refractive index n of the Si layers and of the two layers outside it are shown; the arrowed lines indicate the electric field inside the intrinsic layer.

4.1.2 Cell structure

Different from the crystalline Si solar cell, a p-i-n diode is used for a-Si:H solar cells instead of a p-n diode, which is related to the small (<1 μm) minority diffusion length in an a-Si layer [91, 99]. So the separation of the EHP is by drifting inside the internal field established by the junction voltage between the p- and n-type silicon layers. Detailed analysis of a-Si:H based solar cells have been fully done in many renowned books[1], and here we just give a brief qualitative description of a single-junction n-i-p amorphous solar cell, which we integrate on top of the CMOS chips. Fig. 4.1 shows a schematic diagram.

[1] Chapter 6 of R. E. I. Schropp, and M. Zeman, *Amorphous and microcrystalline silicon solar cells : modeling, materials, and device technology*, Boston: Kluwer Academic, 1998; chapter 4 of A. Shah, *Thin-film silicon solar cells*, Lausanne; Boca Raton: EPFL Press ; distributed by CRC Press, 2010; chapter 13 by S. M. Sze, and K. K. Ng, *Physics of semiconductor devices*, Hoboken, NJ: Wiley-Interscience, 2007.

As shown in Fig. 4.1, the light impinges on the solar cell and passes through the top ITO layer. The light can be further absorbed inside the i-Si layer and converted into electron-hole pair (EHP). If, during the first passage, it is not entirely absorbed in the i-Si layer, it can be reflected back as shown by the yellow arrows and dashed line in Fig. 4.1. (The silicon layers were sandwiched between the ZnO and ITO, with relatively low refractive indexes, n = 2.0, compared to that of the Si layers n = 4.0 [129, 130]). After the light is converted into EHPs inside the intrinsic layer, electrons and holes will be separated by the internal electric field (~1 volt/μm) caused by the junction voltage between n-Si and p-Si layers. Besides collecting the current, the ITO also acts as an antireflection coating, so the thickness will be around 80 to 100 nm, which is around a quarter of the wavelength of the yellow light.

Most of the light absorption and conversion to EHP occurs in the amorphous intrinsic layer. To effectively absorb most of the visible light, the i-layer needs to be several micrometers thick. However, the light trapping by ZnO, ITO and the back reflector effectively increase the length that the sunlight will travel in the i-layer, so the thickness of the i-layer can be between 200~400 nm [91, 128].

A hydrogenated microcrystalline (μ-Si:H) layer is more easily doped and it is also more transparent than an a-Si:H layer [131, 132]. The n- and p-Si layers are normally thin μ-Si:H layers. Their thickness is less than 40 nm to avoid the light absorption inside them, because the EHP generated there will likely recombine within the layer, thus not contribute to the current.

4.1.3 Advantages of a-Si monolithic integration for energy harvesting

As already mentioned in Section 3.1, a-Si:H solar cells have proven fabrication technologies and good indoor light efficiency. Besides that, they offer more advantages: abundant materials (only Si and Sn or Zn are needed for the simplest version of a single-junction a-Si solar cell); environmental friendliness (no Cd, Pb); wide temperature process window (100-300 °C) to offer the device quality a-Si:H; and the strong synergy with flat panel display industry. The IC industry is familiar with the process technology and the transfer of the technology is easier.

4.1.4 Extra challenge for the integration of a-Si solar cells compared to that of a-Si photodiodes

Although there is no pioneering work for integrating a-Si solar cell on top of CMOS, there are a lot of efforts to integrate a-Si photodiodes on CMOS chips, for example, for CMOS based imagers or particle detection. A typical structure of an a-Si:H based CMOS imager is as following: the a-Si:H photo-diode matrix, defined by the pattering of the back electrode, is deposited on the surface of the readout chip, which is an application specified integrated circuit (ASIC). There is an insulation layer between the back electrode and the CMOS circuitry. Such technology has been studied and applied by several groups worldwide, and even led to commercial activities (production of monolithic imagers comprising a-Si:H photodiodes) [133-143].

Although the structure of a-Si:H photodiodes is similar to that of the a-Si:H cells, the solar cell integration is more challenging:

a) The solar cells normally operate at higher pn product, higher current and higher temperatures, the materials choice is critical, both for long term stability and for high efficiency (recombination rate, series resistance).
b) As discussed in Section 3.1, we seek to combine *standard* CMOS with *standard* PV processing, so the engineer's freedom to choose CMOS compatible materials is not presented, so extra efforts must be made to make sure the processes are compatible.
c) As shown in Fig. 4.2, we utilize 100 nm silver layer to enhance the reflection of the light back into the function layer of a-Si solar cells for a higher solar cell efficiency. So silver contamination is a risk that cannot be circumvented through replacing silver by another metal, while silver was not employed in the photodiode works.

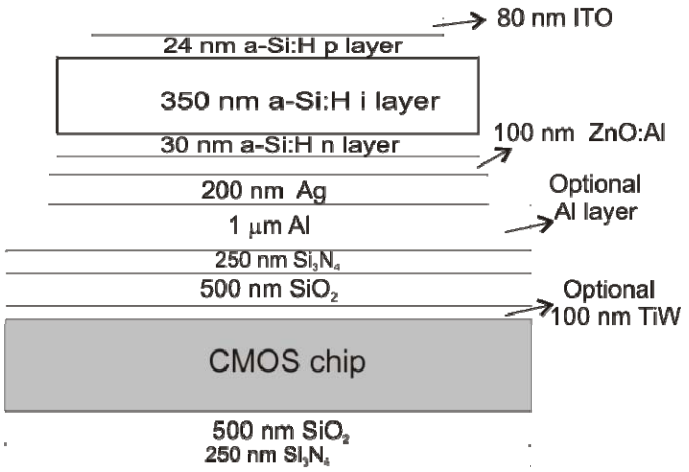

Fig. 4.2. Schematic view of a-Si:H n-i-p solar cell on top of a CMOS chip (not to scale).

4.2 a-Si solar cell integration on CMOS

Two runs of the experiment have been carried out for solar cell integration, which will be indicated as 1st Run and 2nd Run, respectively. For both runs, the experimental approach consisted of six steps:

1) Electrical pre-test of the CMOS chips;
2) Deposition of chip protection films (i.e., passivation layers, see Section 3.2);
3) a-Si Solar cell deposition on CMOS chips by established process flow developed for a-Si solar cell deposition on glass;
4) a-Si solar cell characterization;
5) Removal of the solar cell and the protection films (only for Cu-PCM);
6) Final electrical test of the CMOS chip.

A schematic cross-section view of the realized a-Si:H n-i-p solar cell on a CMOS chip (i.e. after step 3) is shown in Fig. 4.2. In this section, the sample fabrication is further detailed.

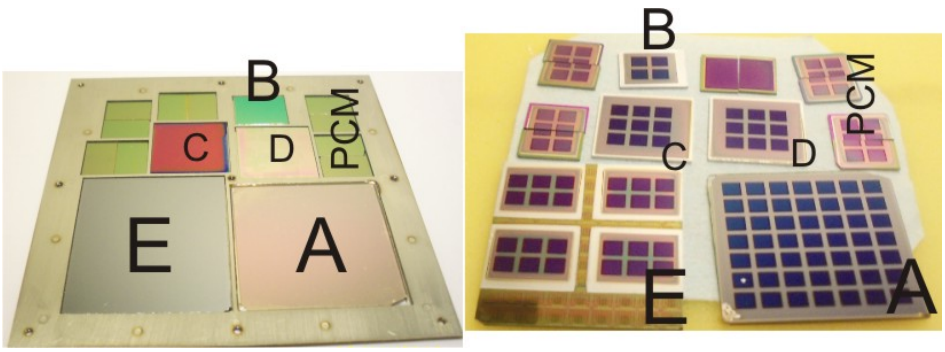

Fig. 4.3. The realized samples with a-Si solar cells. A, B, C, D, E indicate the glass reference plates, Timepix chips, Cu-PCM chips (solar cell made on front side), Cu-PCM chips (solar cell made on backside), and Ringo chips, respectively. PCM stands for other process control module chip. The patterning is realized by stainless shadow mask.

The steps mentioned above were carried out for all the three generations of CMOS chips mentioned in section 3.1.3, in order to investigate the generic applicability of our integration approach to a-Si:H solar cell monolithic integration. For a reference, the solar cells were also deposited on a surface-textured Asahi U-type SnO:F-coated glass.

To make a fair comparison, a sample holder (left of Fig. 4.3) was designed to fabricate the solar cells on all three CMOS chips and the glass reference in the same run, with the same process conditions. Normally, the integration is done on Chips' front side; however, one Timepix, one Cu-PCM chips in the 1st Run and one Cu-PCM chip in the 2nd Run were positioned upside down, to deposit solar cells on the back side of chips. The sample holder including samples and the final devices are shown in Fig. 4.3.

4.2.1 Planarization of the chip surface

The glass plates employed in conventional solar cell production have a well-chosen surface roughness. A slightly textured surface is used, as it aids in the in-coupling and scattering of incoming light. However, an excess roughness will lead to problems with step coverage of the thin film stack [144, 145].

The interconnect of CMOS chips is normally planarized, except for the uppermost layers. Topography exists due to the upper metal layer and the patterned scratch protection layer. We found that the topography on unpre-

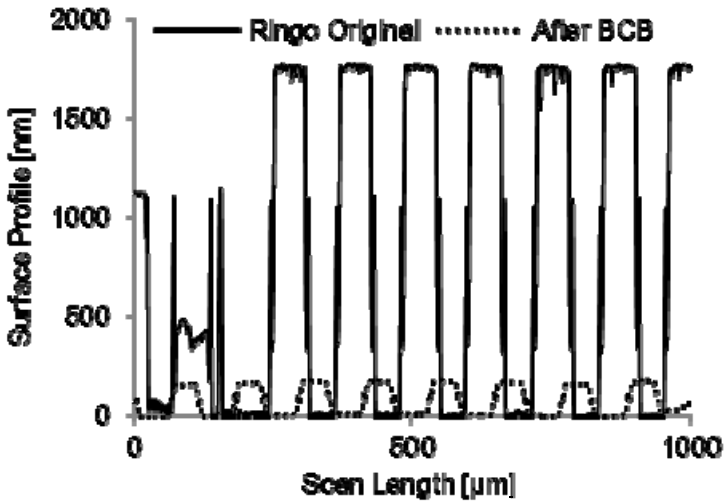

Fig. 4.4. Surface profile of the Ringo chip before and after the BCB polymer planarization layer.

pared CMOS chips is too high to be neglected. Considerable topography is also found on the chips' back side, depending on the pretreatment (such as backlapping).

The integration of a-Si solar cells on Timepix and Cu-PCM chips showed no direct impact of roughness on the solar cell efficiency during the 1st Run experiment [146], but the Ringo chips exhibited even higher topography (see Fig. 4.4). Therefore, we chose to planarize the Ringo chip surface by BCB (benzo-cyclo-butene) [147]. Around 2.8 µm BCB was spin-coated, then cured in a varying-temperature process peaking at 350 °C. A surface profilometer measurement on the Ringo chip before and after planarization is shown in Fig. 4.4. Sufficient planarization is achieved, as later confirmed from PV performance measurements (section 4.3.2).

4.2.2 Passivation layer deposition

Before the solar cell integration, a proper passivation layer needs to be applied to the chip surface, to prevent the chips from a possible damage or contamination.

The process for passivation layer was similar to that described in Section 3.2, but the thicknesses of the layers changed by varying the deposi-

tion time: 500 nm PECVD SiO_2 and 250 nm PECVD Si_3N_4 were sequentially deposited on top of the CMOS chips, then another optional 100 nm SiO_2 can be used to increase the adhesion of the solar-cell bottom electrode. On the back side of the chips, only the SiO_2 and Si_3N_4 layers were deposited.

The deposition of these layers did not affect the underneath CMOS chip, as verified in dedicated experiments in section 3.2. After the chip passivation, 1 μm of Al was further deposited as a part of the bottom electrode of the solar cells.

4.2.3 Solar cell deposition

The a-Si:H solar cells were realized at Utrecht University (UU) using a well-established process, detailed in [59]. Briefly, the a-Si:H cell fabrication comprised the following steps. First, 200 nm of Ag and 100 nm of ZnO:Al were deposited by means of RF magnetron sputtering, using a multi-target sputter tool. Second, n-, i-, and p-type a-Si layers were sequentially deposited by PECVD in a multi-chamber system [148]. The silicon layer thicknesses were 30 nm, 350 nm and 24 nm, respectively. During the deposition, the processing temperature did not exceed 200 ºC. Finally, an 80 nm thick ITO layer was RF sputter-deposited as the solar cell top electrode.

After the 1st-Run experiment, as reported in work [146], three process adaptations were made in the 2nd-Run experiment: the p-type Si layer is now microcrystalline rather than amorphous; the realized samples were optionally annealed at 140 °C in N_2 ambient for 16 hours; and the optional Au grid mentioned in [146] has not been employed for the new experiments, at the expense of solar cell efficiency, for a better comparison. In addition, the active area of the realized solar cells in the 2nd Run is 0.16 cm^2 for all the samples.

Fig. 4.5 shows a cross-section image of a realized solar cell on a Timepix chip, where the image was obtained with a helium ion microscope [149]. Images taken from the glass reference cells confirm that the layers are structurally similar.

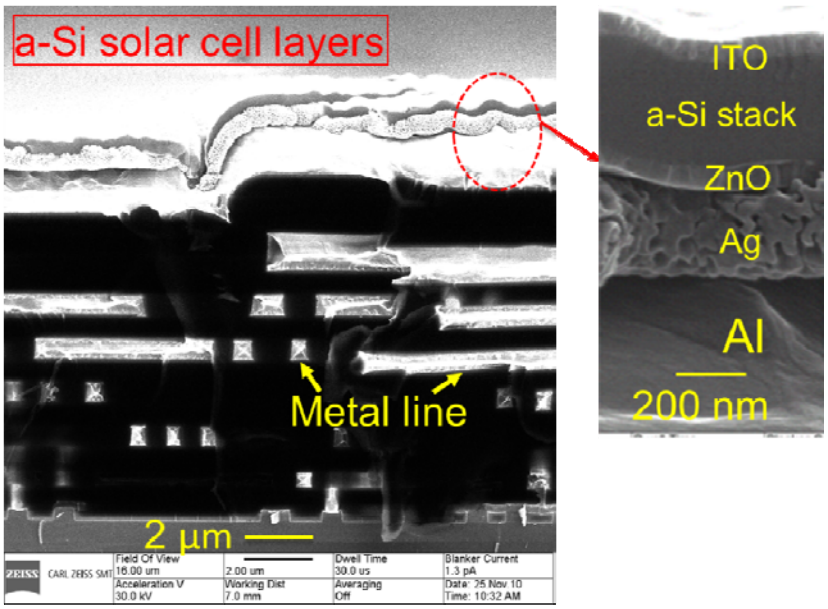

Fig. 4.5. Helium ion microscopy of an a-Si solar cell fabricated on top of the Timepix chip. The metal lines of the CMOS chips and the layer by layer structure of the a-Si solar cell on top of the chip can be seen.

4.2.4 Solar cell de-processing

After the current density - voltage (*J-V*) characterization of the integrated solar cells, for Cu-PCM chips, which needed the electrical characterization again, all the functional and passivation layers were removed to open the bond pads and enable electrical testing of the underlying devices (MOSFETs, MOS capacitors).

For de-processing, HCl solution was used to remove the ITO, ZnO:Al and Ag films; 25% TMAH solution was applied for etching the a-Si:H layers; Buffered-HF was used for removing SiO_2 and Si_3N_4; phosphoric acid (85%) was applied to remove Al metallization and hydrogen peroxide solution was used to remove the TiW.

On the Timepix and Ringo chips, the solar cells can be kept during CMOS re-testing, because the solar cells are deposited away from the relevant bond pads using a shadow mask.

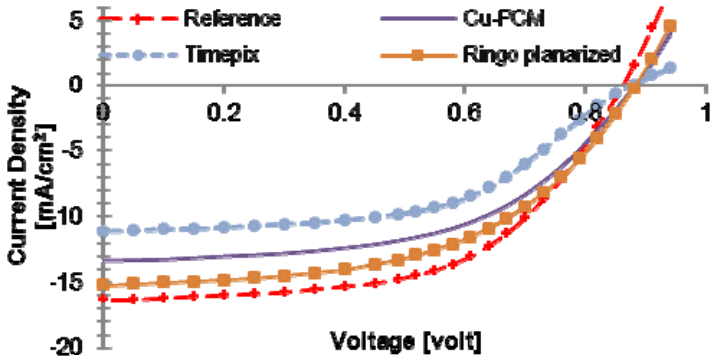

Fig. 4.6. *J-V* curves of solar cells with the highest efficiency on the reference sample and on different CMOS chips under AM 1.5 illumination. All solar cells were integrated on the chip's front side. The *J-V* curve of the Timepix chip from the 1st Run, the others are from the 2nd Run.

4.3 Experimental results

In this section, we present the solar cell performance, including the solar cell efficiency and the yield.

4.3.1 PV cell functionality

The *J-V* measurements have been done at UU to characterize solar cells on the reference glass substrate and on the CMOS chips. The measurements were performed under 100 mW/cm^2 Air Mass (AM) 1.5 condition.

Fig. 4.6 shows the *J-V* curves of the solar cell with the best efficiency on the glass-reference cell and solar cells integrated on the front-side of different generation CMOS chips. Fig. 4.7 shows the *J-V* comparison of a solar cell integrated on the same type CMOS chip. From the *J-V* curves, the important parameters, related to the photovoltaic performance of the solar cells, were extracted and listed in Table 4.1.

In Fig. 4.6, it is seen that the current density of the solar cell on glass and on CMOS shows proper exponential increase with the bias voltage [96]. From Fig. 4.7, one can see that *J-V* curve from the 2nd Run has no *S*-shape around open voltage (V_{oc}) any more compared to the 1st Run. This indicates the new process using a microcrystalline silicon *p*-layer and an anneal at 140 °C in N_2

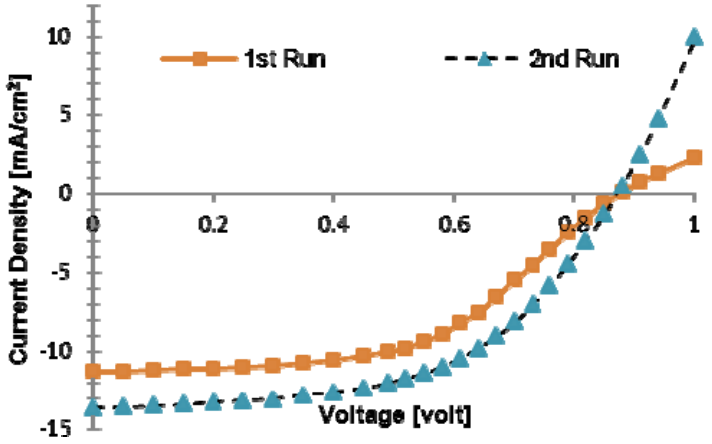

Fig. 4.7. *J-V* comparison under AM1.5 illumination between the 1st Run and 2nd Run solar cell experiment. For both runs, the a-Si solar cells are integrated on the backside of the Cu-PCM chip. *J-V* curve from the 2nd Run has no *S*-shape around open voltage (V_{oc}) any more compared to the 1st Run.

Table 4.1: Parameters of a-Si:H solar cells on different substrates (all the measurements are done under AM 1.5 illumination and all the cells have an active area of 0.16 cm^2). For comparison, the first four samples are from 2nd Run, and the last two rows show the results from the 1st Run.

Samples	Efficiency	J_{sc} mA/cm^2	V_{oc} V	FF	R_s Ω cm^2	R_p Ω cm^2
Glass	7.9%	16.4	0.86	0.56	12	623
Ringo chip pla-narized	7.1%	15.2	0.88	0.53	14	756
Cu-PCM chip front-side	6.4%	13.4	0.88	0.54	16	784
Cu-PCM chip, backside	6.4%	13.6	0.87	0.54	16	837
Cu-PCM chip, backside 1st Run	5.2%	11.3	0.88	0.52	44	1324
Timepix, front-side 1st Run	5.2%	11.1	0.88	0.54	41	748

Note: the symbols are listed and explained in Section 3.1.2.2, where basic theory of the solar cell was described.

can guarantee an Ohmic contact between the functional Si layers and the ITO electrode.

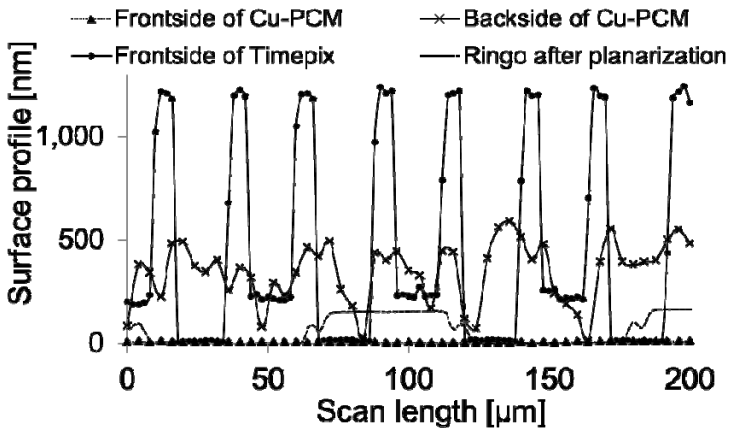

Fig. 4.8. Surface topography of as-fabricated different-type CMOS chips, measured by a profilometer.

The improvement of the electrical properties of the contacts is confirmed by the fact that the series resistance (R_s) of the solar cells in the 2nd Run is 16 Ω·cm^2 (see Table 4.1), less than half the value obtained in the 1st run. The reduction of series resistance is the main contribution of the efficiency improvement of the 2nd Run.

Table 4.1 shows that the solar cell efficiency can be well above 5.0% on different generation CMOS chips. For the BCB-planarized Ringo chips, 7.1% efficiency is achieved. The efficiency gap between glass and CMOS can be less than 1.0% (BCB planarized). The 1.0% gap may be due to that the glass substrate in our experiment have an optimized surface texture [91]: the surface texture can enhance the light trapping, more EHPs will be generated, thus a higher current. Indeed from 2nd column of Table 4.1, we can see that the short circuit current (J_{sc}) on glass is higher than that on CMOS chip.

4.3.2 Solar cell efficiency and yield

As discussed in section 4.2.1, the surface profile amplitude of the CMOS chip is different from that of the glass substrate. The surface profile amplitudes for the used CMOS chips are shown in Fig. 4.8, and Solar cells' best efficiency as a function of the surface profile amplitude is shown in Fig. 4.9. The efficiency of a-Si solar cells is not influenced by surface profile amplitude, indicating good step coverages of all solar-cell thin film layers.

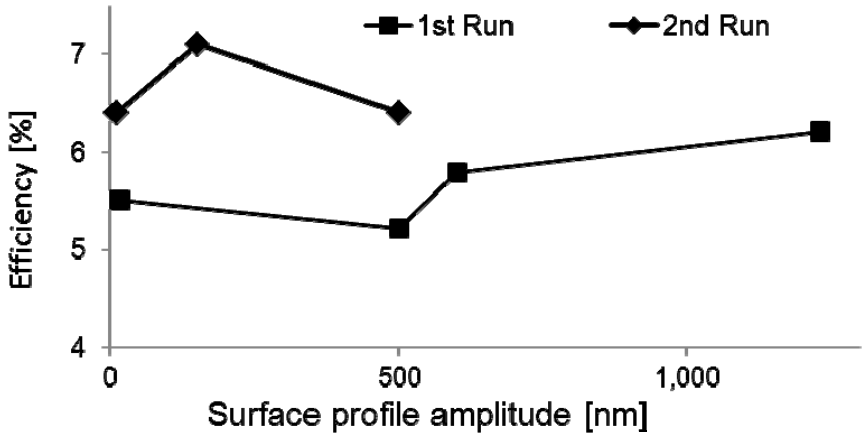

Fig. 4.9. Efficiency of a-Si:H solar cells deposited on CMOS chips with different surface topography. In both the 1st Run and the 2nd Run, the a-Si:H solar cells maintain its efficiency on a very rough surface.

Table 4.2: Yield of a-Si solar cells integrated on top of CMOS chips of different surface amplitude from the 1st and 2nd Run. We consider a solar cell as bad if its efficiency is below 3%.

Substrate	# cells tested	Surface profile amplitude (nm)	Yield 1st run	Yield 2nd run
Glass	49	250	75%	92%
Ringo	24	150	No data	92%
Cu-PCM backside	9	500	44%	89%
dummy	16	700	19%	No data
Timepix frontside	4	1230	25%	0%

Note: The solar cells from 1st Run on glass have an active area of 0.13 cm^2, the others have an active area of 0.16 cm^2.

It is well known that the solar cell yield is related to the substrate roughness [150]. In Table 4.2, the solar cell yield is summarized. It is clear that, if the surface profile amplitude is less than 500 nm, the yield is hardly influenced. However, for a profile larger than 1 μm, the yield drops down to 25%. The yield of the BCB-planarized samples reached 92%, and is close to that of the textured-glass reference cell. This result also coincides with findings in [150].

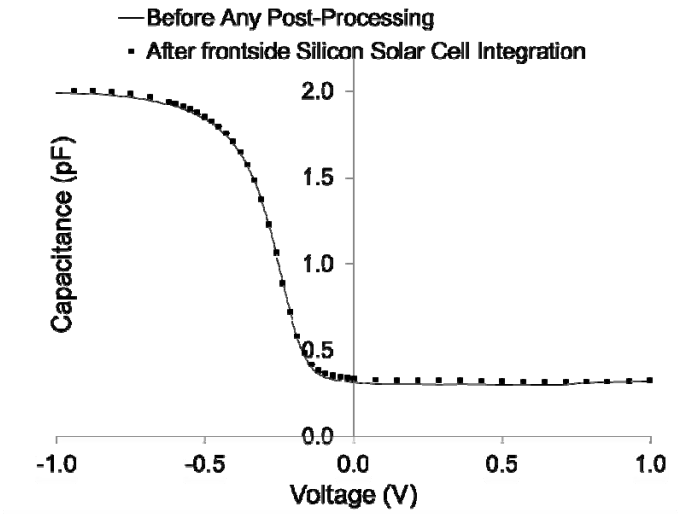

Fig. 4.10. Typical *C-V* curves of a MOS capacitor before and after a-Si:H solar cell integration on the chip's front side (Data from 1st Run).

4.4 CMOS compatibility of a-Si Solar cell Integration

In this section, the CMOS functionality after a-Si solar cell integration is addressed. Capacitance-Voltage (*C-V*) and current-voltage (*I-V*) measurements are reported on the Cu-PCM chips, followed by tests of the functionality of CMOS ring oscillators and a full mixed-signal CMOS circuit (Timepix).

4.4.1 C-V and I-V measurements on the Cu-PCM chips

The capacitance-voltage (*C-V*) curves of MOS capacitors and the current-voltage (*I-V*) curves of MOS transistors were measured before and after the solar cell integration, using a Keithley 4200 SCS at the University of Twente.

The MOS capacitor area was 1.44×10^{-6} cm^2 with a gate oxide thickness of 2.2 nm. All the capacitance measurements were carried out at a frequency of 1 MHz. The MOSFET has a gate length of 130 nm. The drain-source voltage was 1.0 V and the source and body were connected to ground for the transistor measurements.

As discussed earlier, a-Si solar cells can be integrated on front-side or back-side of the Cu-PCM chip, and the electrical characterization has been done for

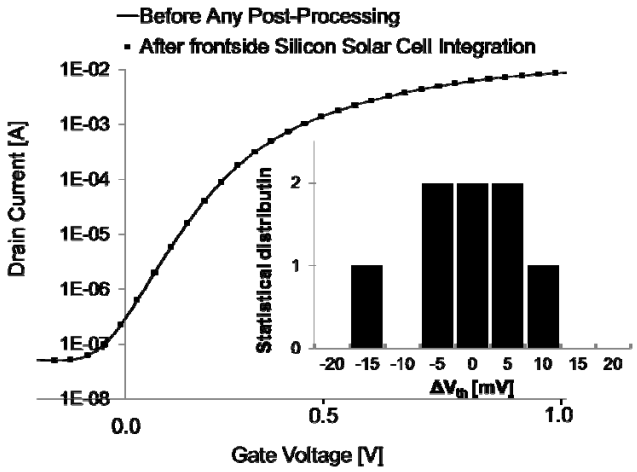

Fig. 4.11. *I-V* curves of an NMOS transistor before and after the same post-processing. The inset shows the threshold voltage shift statistics of 8 transistors. (Data from 1st Run)

Table 4.3: MOSFET parameters before and after a-Si:H solar cell integration on the chip's front side (values averaged over 8 transistors).

	Before Processing	After solar cell integration	Absolute change	Relative change
I_{leak} (μA)	17.11	17.16	0.05	0.2%
I_{on} (mA)	8.21	8.39	0.19	2.5%
I_{off} (nA)	745	744	1	0.1%
V_{th} (mV)	-127	-122	5	3.9%

both cases. Almost identical performance has been observed for both, so only the results of the front-side integration are shown here.

There is no visible difference in the *C-V* curves of MOS capacitors and the *I-V* curves of the MOS transistors before and after the solar cell front-side integration, as seen from Fig. 4.10 and Fig. 4.11.

From the *C-V* and *I-V* curves, the key performance parameters were derived: the gate leakage current and drain saturation current (I_{leak} and I_{on}, respectively, both obtained at $V_{GS} = 1$ V), off current (I_{off}), threshold voltage (V_{th}), and subthreshold swing (*S)*. The values averaged over 8 transistors are shown in Table 4.3. After the solar-cell integration, changes of all the parameters are small. The most significant shift is observed for the threshold voltage of the front-side integrated solar cells. The absolute average value of this change

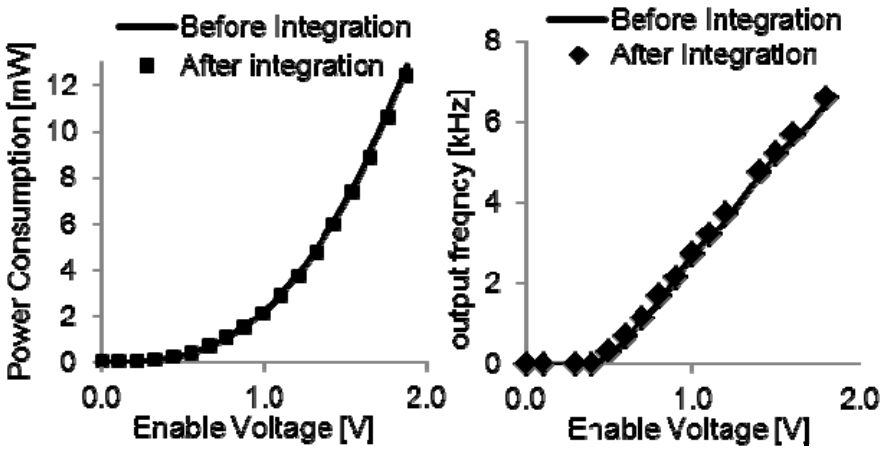

Fig. 4.12. Power consumption (left) and the output frequency (right) versus enable voltage of the Ringo before and after the a-Si solar cell integration. The Ringo is read out via an embedded 512 times frequency divider. Experiment data are from 2nd Run.

(~5 mV) is quite acceptable in view of similar V_{th} shifts encountered after conventional packaging processes [151].

4.4.2 Functionality of a CMOS Ring Oscillator

A ring oscillator is widely used as a tool to characterize CMOS performance [152]. In our experiments, the power consumption and the output frequency versus the enable voltage of a 17-stage ring oscillator have been measured before and after the solar cell integration by Keithley SCS 4200 and Agilent/HP 54642A oscilloscope. The ring oscillator includes a 512 times divider to reduce frequency at the output. The results are shown in Fig. 4.12.

One can observe that there is no significant impact of the integration on the ring oscillator (Ringo) performance both in terms of its power consumption and oscillating frequency.

4.4.3 Functionality of the Timepix chip

The Pixelman software [117] and an automated probe station were employed for functional testing of the Timepix chips at the Nikhef Institute in Amsterdam (NL). The software will test the functionality of analog CMOS circuitry arranged in 256 columns of 256 pixels. Each pixel contains 550

Table 4.4: Digital and analog test results of the Timepix chip before and after a-Si:H solar cell integration on the chip's front side.

	Digital Testing		Analog Testing	
	Bad columns (out of 256)	Bad pixels (out of 65536)	Bad columns (out of 256)	Bad pixels (out of 65536)
Before integration	8	2127	9	2875
After integration	9	2258	12	4578

transistors. As mentioned in Section 3.1.3 already, the post-processed chips were of a lower-quality category than those normally used. A fraction of the pixels and columns therefore malfunctions before solar cell integration. A summary of the test results is presented in Table 4.4.

The number of bad columns for both the digital and analog test increased marginally; 98.8% of the chip pixels were unaffected by the solar cell integration. The change is insignificant according to Timepix test experts[153], on the basis of test repetition experience. Similar to the the findings with Cu-PCM and Ringo chips, the Timepix results indicate the possibility of post-integrating solar cells above standard CMOS circuits.

4.5 Conclusion

In this chapter, we discussed the successful integration of a-Si:H n-i-p solar cells on CMOS chips by post-processing. The solar cells on-chip showed an efficiency around 7.1% under AM1.5 irradiation conditions. This efficiency is comparable to that of the glass reference, and may be further increased by texturing the underlying CMOS or the solar cell's bottom electrode. The cell yield is equally high on glass and on BCB-planarized CMOS.

For post-processing, we used unpackaged CMOS chips of three generations. Results are presented on 0.13-µm (Cu-backend) CMOS microchips with PCM test structures, 0.18-µm-technology (Al-backend) 17-stage ring oscillators and 0.25-µm (Al-backend) CMOS integrated circuits (Timepix). All three microchips showed unaffected CMOS performance after post-processing.

Chapter 5. CIGS Solar cell integration as energy harvester

In this chapter, we consider the monolithic integration of copper indium gallium (di)selenide CIGS solar cells on deep-submicron CMOS microchips using a similar experimental approach as presented for the a-Si cells in chapter 4. The chapter starts with a brief introduction to CIGS solar cells, followed by discussion of the integration challenges (Section 5.2) and the process integration scheme (Section 5.3). Photovoltaic performance is documented in Section 5.4; CMOS performance in Section 5.5, followed by the Conclusions.

5.1 Introduction to CIGS solar cell

5.1.1 Brief history

$Cu(In_{1-x}Ga_x)Se_2$ (CIGS) is a semiconducting I-III-VI_2 compound with chalcopyrite crystal structure [154]. CIGS-based solar cell research started almost at the same period as for a-Si:H-based solar cells, both perhaps due to the oil crisis in the 1970s. In the past 30 years, CIGS-based solar cells changed dramatically. Fig. 5.1 shows the schematic representation of the first CIS-based solar cell and that of the state of the art technology.

In 1975, J.L. Shay, Sigurd Wagner, *et al*., from Bell Labs [154, 155] reported the first CIGS-based solar cell with a 12% efficiency under 71 mW/cm^2 illumination[1]. The 5~10 μm thick CdS was thermally evaporated onto a single crystal p-type $CuInSe_2$ (CIS)[2], and Au and In were the contacts to CIS and CdS, respectively.

In 1980, Mickelsen, et al., from Boeing Co. first reported the polycrystalline CIS solar cell with a 5.7% efficiency under 100 mW/cm^2 solar light illumination [157]. They used a patented two-stage simultaneous elemental thermal co-evaporation. In 1988, Mitchell, et al., from Arco solar Co. reported 14.1% efficiency (100 mW/cm^2 illumination) for a polycrystalline CIS solar cell.

[1] The AM 1.5 solar spectrum standard was set by American Society for Testing and Materials (ASTM) in June 1999, so before that different solar spectrum might be used.

[2] Shay, *et al*., don't specify the thickness of the CIGS layer, but it should large than 10 μm according the contents inside the paper.

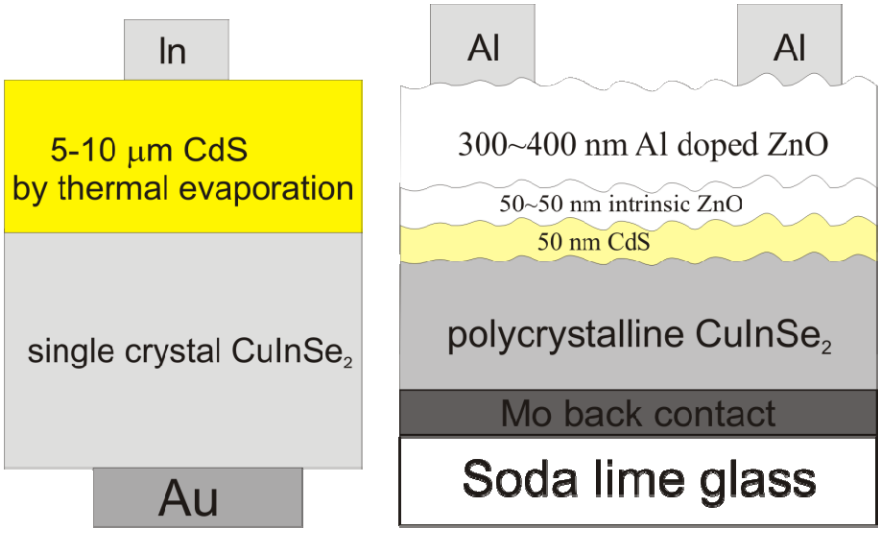

Fig. 5.1: Schematic diagram of CIGS based solar cells. Left, the layer structure of the first reported CIS solar cell [154, 155]; right, the layer structure of the state of the art CIGS solar cell technology [156]

The technology was later reported as selenization of the sputtered stacked CuInGa metal precursor layer in H_2Se [158].

During 1980s, researchers also made three important developments. First they switched from pure CuInSe or $CuGaSe_2$ [159] to $CuIn_{1-x}Ga_xSe_2$, where x is between 0.25 to 0.27 [158, 160, 161]. Second, the efficiency was increased to more than 14% by replacing a thick (several micrometers) sputtered CdS by a combination of a thin chemical-bath deposited CdS and an RF-sputtered ZnO and Al:ZnO layer stack [158, 162-165]. Third, incorporation of sodium into the CIGS solar cell can improve the efficiency due to an improved film morphology, a higher conductivity and other beneficial effects, which was first identified by Stolt, Schock, *et al.* [163].

In 1994, another breakthrough came: Gabor, Contreras, Noufi and their colleagues from National Renewable Energy Laboratory USA (NREL) reported a record efficiency of 15.9% for CIGS solar cells based on a three-stage co-evaporation process [166]. Fig. 5.2 shows the time-temperature profile of the three-stage co-evaporation process. Later, a lot of research studies have been done based on this process technology [167-169]. The CIGS efficiency approached 20% by the end of last century [170].

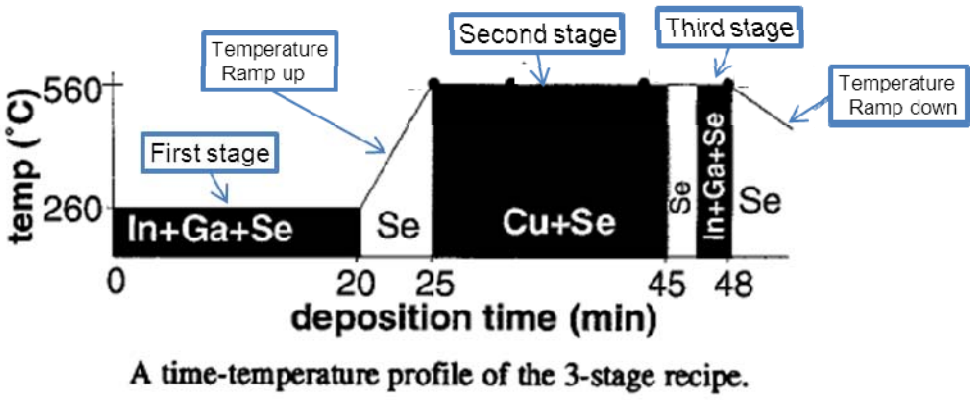

Fig. 5.2. Thermal profile versus time for the 3-stage CIGS deposition. The 19.9% efficiency CIGS solar cells from NEREL were fabricated based on this process flow [156]. Data sources are from [171].

By the year of 2011, the world record laboratory CIGS efficiency is 20.3±0.6% obtained by ZSW (Germany) by modified co-evaporation[1], and the world record module CIGS efficiency is 15.7±0.5% achieved by Miasole Co. by the selenization of the sputtered CuInGa metal precursor layer [22][2].

5.1.2 Basic theory

A CIGS-based solar cell is intrinsically a p-n$^+$ diode with the diode ideality factor between 1.6 and 1.8 [105]. Due to the complexity of CIGS's ternary system, the operating mechanism is still not completely understood, although there were plenty of investigations carried out [172-179]. In the text below, a brief qualitative description of the CIGS solar cell operation is given.

Fig. 5.3 shows the band diagram, and the numerical values related to the figure are listed in Table 5.1, mainly based on the work of Uwe Rau [176, 179]. On top of the Mo back electrode contact, it is the p-type CIGS functional layer. Its energy band gap (E_g) varies from 1.1 to 1.7 eV, depending on the Ga content. For a better top window layer transparency to the solar light, researchers replaced the n-region from CdS to CdS/ZnO/Al:ZnO,

[1] The details of the process have not been disclosed by ZSW, Germany.
[2] The details of the process have not been disclosed by Misole Co, USA.

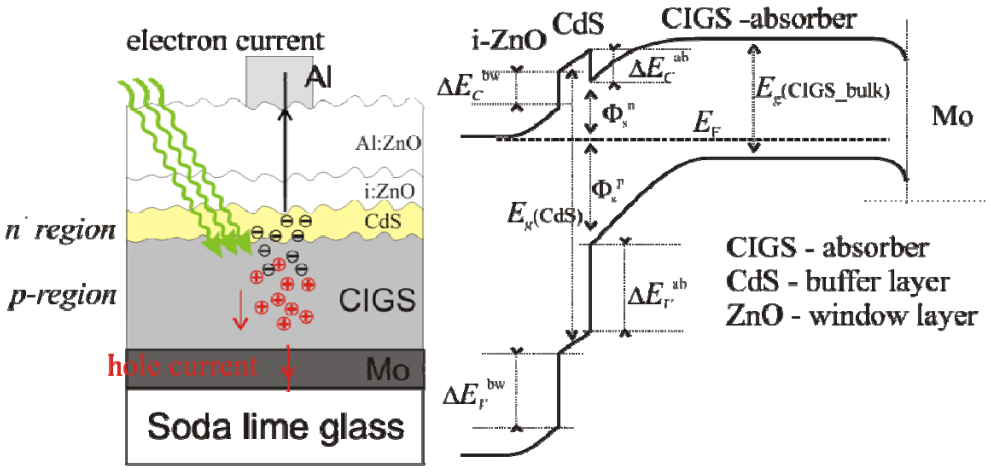

Fig. 5.3. Band diagram of the CIGS solar cells. E_g stands for the band gap; ΔE_V^{ab} and ΔE_C^{ab} stands for the valence and conduction band discontinuities at the **a**bsorber-**b**uffer interface; ΔE_V^{bw} and ΔE_C^{bw} stands for those at the **b**uffer-**w**indow interface; Φ_s^p and Φ_s^n stand for the Fermi potential from valence band edge and Fermi potential from conduction-band edge at the surface of CIGS, respectively. Sources are the works of Uwe Rau [176, 179].

Table 5.1: Numerical values related to the band diagram of the CIGS/CdS/ZnO structure in Fig. 5.3. Data sources are the works of Uwe Rau [176, 179] and page 789 from Sze's book.

$E_g(CIGS_{Bulk})$	$E_g(CdS)$	$E_g(ZnO)$	Φ_s^p	Φ_s^n
1.0~1.2	2.4~2.5	3.3~3.4	0.8	0.6
ΔE_V^{ab}	ΔE_C^{ab}	ΔE_V^{bw}	ΔE_C^{bw}	
0.6~1.0	0.2~0.3	1.2	0.3	

Note: the unit for all the parameters is electron volt

because E_g of CdS smaller than that of ZnO. The thin intrinsic ZnO is necessary to prevent the possible short circuits.

As shown on the left-hand side in Fig. 5.3, the light impinges on the solar cell, passing through the ZnO window and CdS buffer layers. After the conversion of light into the EHPs, they will be separated by the internal electric field due to the junction voltages across the n^+-p region. The hole current will flow towards the Mo back contact; the electron current will flow to the top Al electrode.

5.1.3 Integrated CIGS solar cell as energy harvester

As detailed in Section 1.4 of this thesis, the integration of a thin-film solar cell on a microchip may be a compact and powerful solution to the open issue of energy harvesting for autonomous wireless sensor systems ("Smart Dust").

In standard manufacturing processes, the peak process temperature (> 500 ºC [168]) is (just) too high for CMOS interconnect. Related to this high temperature is the issue of thermal expansion mismatch between the solar cell and the substrate, possibly leading to cracks. Last but not least, high-efficiency CIGS solar cells require a sodium concentration more than 0.5% in the active layer [180, 181], whereas sodium is known to be a most detrimental contamination in CMOS devices [96]. So the monolithic integration of CIGS on CMOS is more challenging than that of a-Si integration. The integration issues will be detailed in the next section, i.e., Section 5.2.

However, good reasons exist to pursue CIGS monolithic integration. Of all single-junction thin film solar cells not employing a monocrystalline semiconductor, CIGS cells exhibit the highest cell efficiency (20.3±0.6%) and module efficiency (15.7±0.5%) among all single-junction thin film solar cells [22]. The band gap of the CIGS solar cell can be tuned between 1.1 and 1.7 eV by varying the Ga:In ratio. This allows bandgap tuning for maximum efficiency at the indoor light spectrum. The efficiency at indoor light is reportedly larger than 5% [23, 105]. Last but not least, very good long-term reliability and radiation hardness are further reported for this type of thin-film solar cell [182].

The first work on integration of the CIGS material as image detector on top of CMOS was presented in [183]. In this thesis, we present the successful CIGS integration as a solar cell on 0.13-µm, 0.18-µm and 0.25-µm CMOS chips. The microchips maintain comparable electronic performance after the integration and the solar cells on top show an efficiency of 8.4±0.8% and a yield of 84%, both values close to the glass reference.

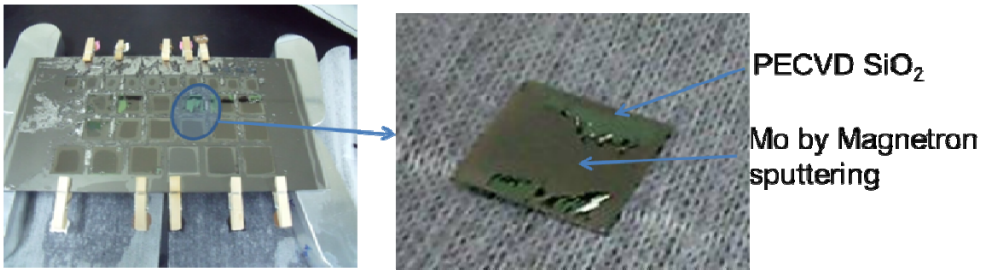

Fig. 5.4: The widely used two-stage Mo deposition process [184], which can have good adhesion between Mo and soda lime glass, cannot assure good adhesion between Mo and the PECVD passivated CMOS chip.

5.2 The CIGS integration Challenge

For the final microsystem, we want the PV efficiency as high as possible, and the CMOS chip's functionality unaffected. Five integration challenges must be overcome to achieve these goals.

First, good adhesion between the solar cell and the underlying CMOS chip is a necessity. The first PV layer on glass plates is molybdenum. As shown in Fig. 5.4, we found Mo deposited by the standard 2-stage magnetron sputtering [184] can have good adhesion on glass, but adheres poorly on our CMOS chips (using only wet cleaning as surface preparation). We found that, a 10-nm titanium (Ti) layer deposited prior to Mo deposition can resolve this problem. The resulting layers passed the Scotch tape test [185].

Secondly, copper is a compulsory element in CIGS solar cells, and sodium is necessary for higher efficiency. However, these metals exhibit fast diffusion coefficients in intermetal dielectrics and silicon, and are active as mobile charge and as bandgap defects [96, 186]. Hence a diffusion barrier must be administered between the microchip and the solar cell. Si_3N_4 is widely used as diffusion barrier layer against mobile ions [187], and in our experiments, we have employed 300 nm PECVD Si_3N_4 to this purpose.

Third, the standard CIGS solar cell processing involves necessary plasma processes, which may cause plasma charging damage to the underlying transistors [188]. It is however known that a 150-200 nm dielectric layer can block the possible plasma charging damage [189], hence the diffusion barrier layer mentioned above serves a second purpose.

The peak process temperature is a fourth concern. The highest CIGS efficiencies are obtained using process temperatures of 500-550 °C [156]. CMOS backend interconnect, particularly Al-based interconnect, cannot withstand such temperatures, leading to crack voiding, hillock formation and corrosion [190]. Some CIGS literature however reports quite good solar cell performance at reduced processing temperature in the range of 310-450 °C [191-193].

Finally the added solar cell layer may have intrinsic stress which will be imposed on the underneath CMOS circuits, thus influencing the performance of the chip [151, 194]. CIGS experiments on a variety of substrates have shown that the mismatch in thermal expansion between substrate and CIGS can lead to CIGS adhesion problems and the cracking of Mo [191].

The Mo-adhesion issue can be monitored by visual inspection combined with a Scotch tape test. Proper photovoltaic performance and unaffected CMOS functionality are the best evidence of the resolution of the other four issues, as detailed in Sections 5.4 and 5.5.

5.3 Prototype design and experiment

In Fig. 5.5, a schematic cross-sectional view of a CIGS solar cell, integrated on the front side of a CMOS chip, is shown. The solar cell can also be integrated on the backside of the chip.

The experimental approach is as that of a-Si solar cell integration: after the CMOS electrical characterization, the chips were passivated, followed by the conventional CIGS solar cell process. The CIGS solar cell integrations were done in the CIGS group of Nankai University chaired by Prof. Sun Yun.[1] After the PV characterization of the realized solar cell, the solar cell stack and the passivation layers were removed from some of the CMOS chips in order to test the underlying CMOS chip again.

The solar cells are deposited on glass reference plates (soda-lime glass in this case), the 0.13-μm CMOS chips containing Process Control Modules

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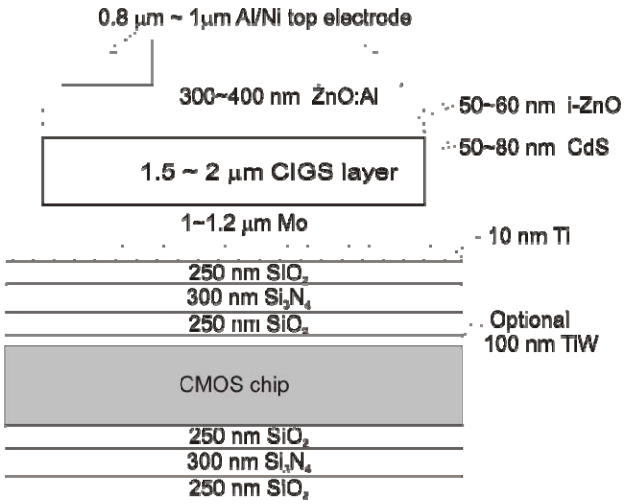

Fig. 5.5.Schematic view of a CIGS solar cell fabricated on top of a CMOS chip (not to scale). The 100 nm TiW layer is only applied to Cu-PCM chips as an etch-stop layer. A 10 nm Ti is administered between the top SiO_2 and the bottom Mo electrode for better adhesion in the 2nd Run. In these experiments, no interconnection was made between solar cell and CMOS.

(labeled Cu-PCM), 0.18-μm CMOS chips containing ring oscillator structures (labeled Ringo), and 0.25-μm CMOS chips with a fully functional 1.6×1.4 cm^2 mixed-signal CMOS circuit [110] (labeled Timepix). For a detail description of the CMOS chips, see Section 3.1.3.

Different from the a-Si solar cell integration presented in Chapter 4, no BCB planarization was utilized before passivation, because BCB cannot withstand the high temperature of the CIGS solar cell process.

Two successful experiments have been carried out, and we will use the 1st Run and the 2nd Run to denote them, respectively.

5.3.1 Passivation layer deposition

As discussed in Section 3.2, before the solar cell integration, a passivation layer is deposited on the chip surface. The layer stack consists of 250 nm SiO_2, 300 nm Si_3N_4 and 250 nm SiO_2 deposited by plasma enhanced chemical vapor deposition (PECVD) at 300 ºC. By scotch tape testing comparisons, it was found that the upper layer of SiO_2 leads to much better adhesion of the following Mo layer than Si_3N_4. After the chip passivation, the chips are annealed at 425 ^oC in N_2 ambient to release the abundant H_2.

For Cu-PCM chips, a thin (100 nm) TiW layer is added underneath, acting as an etch-stop layer for deprocessing the stack later on without affecting the CMOS upper layers.

5.3.2 Solar cell deposition

The CIGS solar cells were realized using the three-stage co-evaporation process documented in [166, 168, 195]. First, 1-1.2 μm of Mo is deposited by magnetron sputtering. For the 2nd Run a 10 nm sputtered Ti layer is inserted for good Mo adhesion, which was not done for 1st Run. After Mo deposition, a 20-30 nm of NaF precursor layer was thermally evaporated in order to supply Na to the following CIGS absorber layer, necessary for efficient CIGS solar cells [180]. After that, the p-type CIGS absorption layer was co-evaporated by the 3-stage method [168] onto the Mo-coated CMOS chips and glass substrate in the same chamber without vacuum break. The n-type buffer layer of CdS was deposited by chemical bath deposition at 80 °C, then 50 nm of intrinsic ZnO (i-ZnO) layer and 300 nm of Al doped ZnO (ZnO:Al) were sequentially deposited by RF magnetron sputtering as transparent window layers. Finally, the nickel-aluminum top electrode grid was thermally evaporated onto the device by shadow mask.

For the 1st run, the finished solar cells have an active area of 0.27 cm^2; for the 2nd Run, the finished solar cells have an active area around 0.29 cm^2.

5.3.3 De-processing of the solar cells

After the characterization of the obtained solar cells, the solar cell layers and the passivation layers on Cu-PCM CMOS chips were removed to expose the bond pads of the test structures. For de-processing, HCl was used to remove the Al-Ni, ZnO:Al and CdS; fuming nitric acid was applied for etching the CIGS absorber layer and the Mo bottom electrode; BHF was used for removing SiO_2 and Si_3N_4; hydrogen peroxide was used to remove the TiW.

5.3.4 Physical characteristics of CIGS solar cell on chip

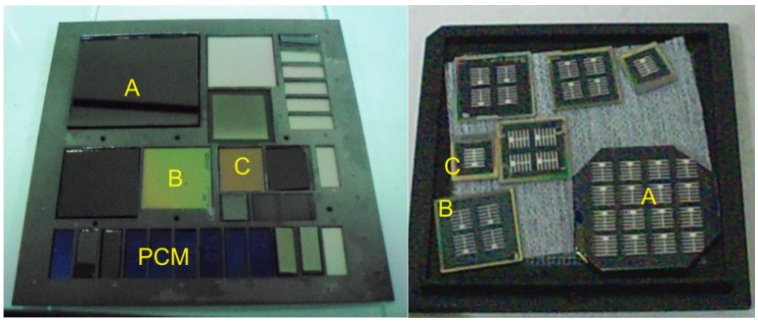

Fig. 5.6: Left: 10x10 cm^2 sample holder for different types of samples for CIGS solar cell deposition experiments. Right: finished samples with CIGS solar cells on top. In both images, A, B, C denote the glass reference plates, Cu-PCM chips and Timepix chips, respectively. Additional PCM samples are included in the same run.

Fig. 5.6 shows the integrated PV cells on different-type CMOS chips and PCMs. On the left-hand side, the chips are visible as mounted into the chip holder prior to post-processing. The right-hand side image shows the samples after solar cell manufacturing.

Fig. 5.7 and Fig. 5.8 show Helium Ion Microscope (HIM) [149] cross-sections of the CMOS chips with solar cells on top. In Fig. 5.7, we can see the metal levels of the Timepix chips, and the layer by layer structure of the CIGS solar cell on top. The CMOS has some topography (approximately 1 µm), as visible from the nonplanar solar cell thin films. The figure suggests that the step coverage of the solar cell layers is sufficient to cope with this topography, but electrical results should give more conclusive evidence in this respect.

Fig. 5.8 illustrates the crystal structure of the Mo, CIGS, ZnO and Al grid. The Mo and CIGS have columnar polycrystalline structure. The grain size of the Mo layer is around 60 nm, as derived from XRD data using the Scherrer equation [196, 197]. The grain size of the CIGS is well above half a micrometer, which can be observed by top-view HIM microscopy. Detailed analysis of these is reported elsewhere [198]. These grain sizes depend on the process conditions [199, 200]. The obtained values are suitable for good CIGS solar cell performance [201].

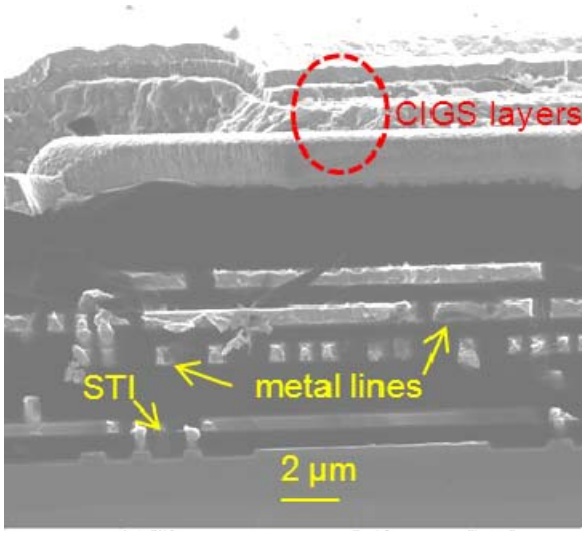

Fig. 5.8. HIM picture of the CIGS solar cell on top of the Timepix. Going from bottom to top, the chip's shallow trench isolation and interconnect are visible, followed by the CIGS solar cell layer stack.

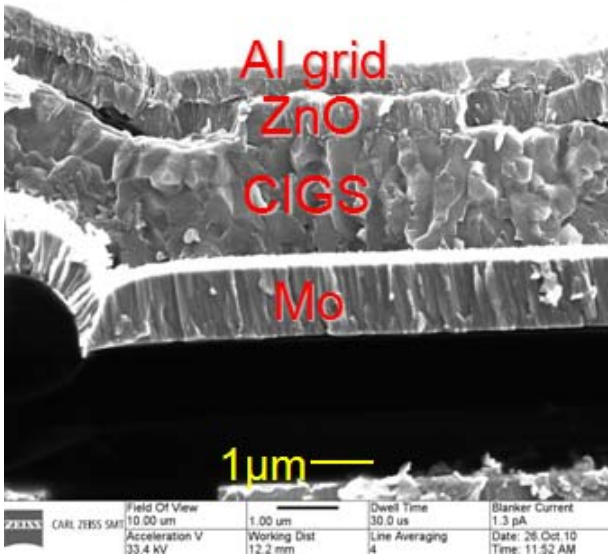

Fig. 5.8. Close-up HIM image of the CIGS solar cell layers on a Timepix chip. The columnar poly-crystalline structure of different layers can be distinguished in the picture.

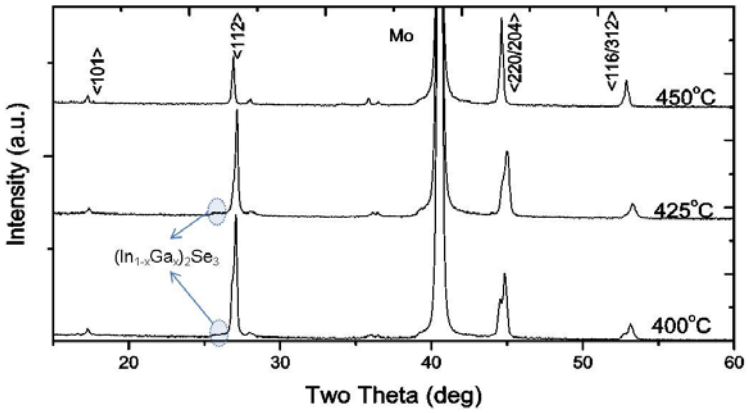

Fig. 5.9. XRD data of CIGS on glass, fabricated at 400 – 450 °C. A shoulder on the left of the peak 2θ = 27° is visible in the 400 °C- and 425 °C-deposited films, however for 450 °C-deposited films, there is no such shoulder indicating the existence of $(In_{1-x}Ga_x)_2Se_3$ phase. For 450 °C, the corresponding $(In_{1-x}Ga_x)_2Se_3$ peak is not present, pointing to an improved film crystallinity.

5.4 Solar cell Experimental results

In this section, we present the solar cell performance, comparing the cells on CMOS with the reference ones on glass. Material properties are compared as well as the current-voltage behavior under light illumination.

5.4.1 Crystallinity and chemical composition of the CIGS layer

The crystallinity and the chemical composition of the CIGS layer of the samples were measured by X-ray diffraction (XRD) and X-ray fluorescence (XRF) analysis, respectively.

From Fig. 5.9, we see in the 400 ºC and 425 ºC fabricated CIGS solar cells an indication of the existence of $(In_{1-x}Ga_x)_2Se_3$. This is commonly attributed to a lack of thermal activation energy, and may result in a reduced solar cell efficiency may result [146, 193]. The <112> peak at 450 ºC shifts to lower number compared to the same peaks at other temperatures. This indicates a lower incorporation of Ga, which can be confirmed by XRF measurement of Ga ratio as shown in the last column of Table 5.2.

Fig. 5.10 shows the XRD data of the CIGS fabricated at 425 °C on CMOS substrate and on glass substrate. Disregarding the peaks from the Si <100> substrate, the diffraction peaks coincide. However, the peak ratio between

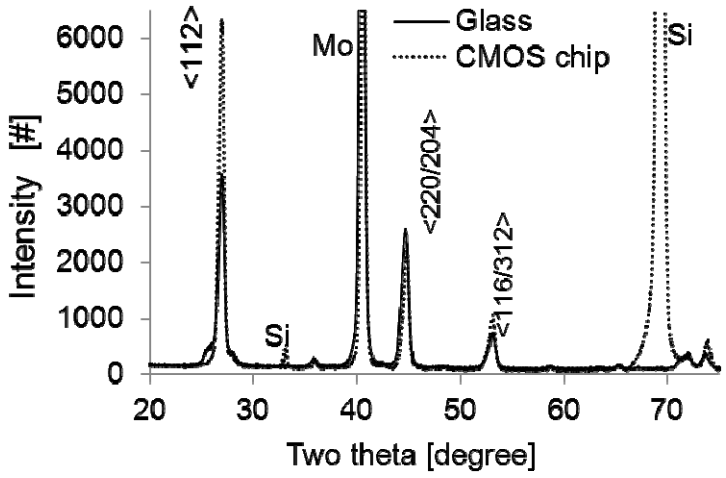

Fig. 5.10. XRD data comparison of CIGS on glass substrate and that on Cu-PCM substrate fabricated at 425 °C in the same run. Except two peaks from the Si <100> substrate, the diffraction peaks from CMOS chip and glass substrate coincide.

Table 5.2: Chemical composition by XRF of CIGS layers deposited on various substrates and at different temperatures.

T (^{o}C)	substrate	Cu (at.%)	In (at.%)	Ga (at.%)	Se (at.%)	Cu/ (In+Ga)	Ga/ (In+Ga)
	Expected	22-24	19-20	6-7	50-51	0.88-0.91	0.25-0.27
400	Glass	22.8	18.7	7.6	51.0	0.87	0.29
	CMOS	22.5	18.0	8.2	51.2	0.86	0.31
425	Glass	22.4	18.9	7.5	51.2	0.85	0.28
	CMOS	23.4	18.5	7.1	51.1	0.84	0.28
450	Glass	23.6	20.8	4.8	50.2	0.92	0.19
	CMOS	22.7	21.5	4.4	50.3	0.87	0.17

<220/204> and the <112> on CMOS is smaller than that on glass, which will result a lower-efficiency solar cell on the CMOS chip (a relatively higher <220/204> peak is preferred for a high efficiency CIGS solar cell) [109, 202].

Table 5.2 shows the atomic chemical composition (at.%) of CIGS on various substrates and deposited at various temperatures. The "expected" row indicates the aimed (i.e., providing best efficiency) composition [202, 203]. In

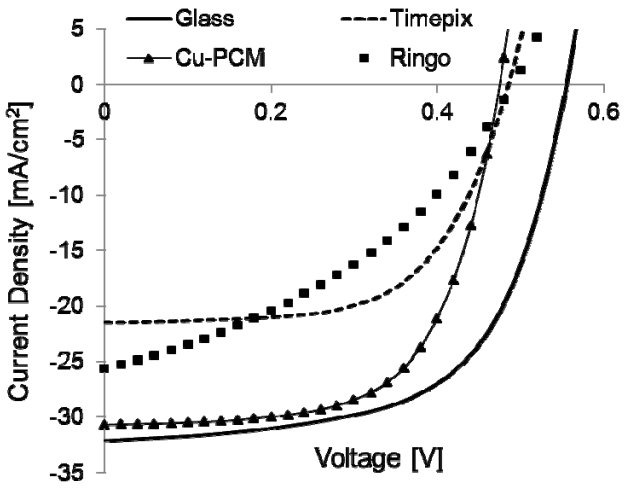

Fig. 5.11. *J-V* curves of the highest-efficiency solar cells fabricated at 425 °C peak temperature, on glass and on different generation CMOS chips, i.e., Cu-PCM (0.13-µm), Ringo (0.18-µm) and Timepix (0.25-µm).

each run (i.e. deposition temperature), the compositions on glass and on CMOS are almost identical and are close to the optimum.

From our comparison of the XRD and the XRF analysis of the CIGS layers, we conclude that an identical crystallinity and chemical composition has been obtained on CMOS and on glass. However, below 450 °C peak deposition temperature, there is a residual $(In_{1-x}Ga_x)_2Se_3$ phase from the first stage of the 3-stage co-evaporation method [168, 193], and a change in the crystal orientation changes; both effects may lead to lower solar cell efficiency.

5.4.2 Current-voltage behavior of the solar cells

Current density-voltage (*J-V)* measurements have been done to characterize solar cells on the reference glass substrate and on the CMOS chips. The measurements were performed under standard solar-simulator illumination conditions: 100 mW/cm^2 (Air Mass 1.5, for definition see the footnote on page 63).

The *J-V* curves of the best-performing PV cells on each substrate types were shown in Fig. 5.11. These samples are processed at 425 °C peak substrate temperature in the same run. From the *J-V* curves, the important parameters characterizing the photovoltaic solar cell performance, were

Table 5.3: Parameters of CIGS solar cells on different substrates at 425 °C peak substrate temperature.

Substrate	η	J_{sc} mA/cm^2	V_{oc} V	FF	R_s Ω cm^2	R_p Ω cm^2
Glass (reference)	10.9%	32.19	0.55	0.61	3.0	238.6
Cu-PCM backside	9.2%	30.74	0.48	0.63	2.8	515.1
Ringo	4.9%	25.65	0.49	0.39	8.0	51.9
Timepix	6.4%	21.48	0.48	0.61	4.2	289.5

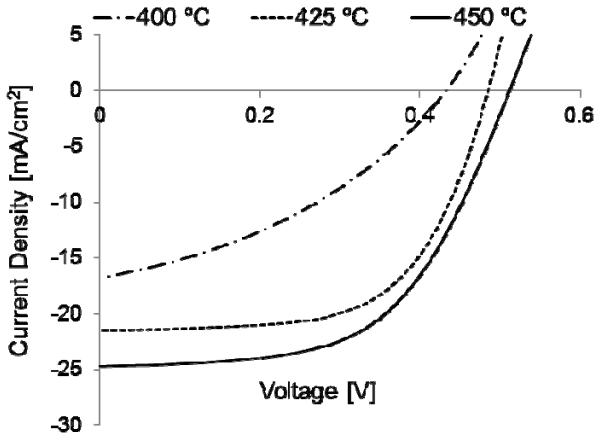

Fig. 5.12. *J-V* characteristics of solar cells on top of the Timepix chip. With increasing deposition temperature, the solar cell performance improves: both J_{sc} and V_{oc} increase.

extracted and listed in Table 5.3. On all types of CMOS chips efficiencies (η) of 4.9% or higher are obtained. The solar cell efficiency on Cu-PCM chips approaches that on glass.

All three chips in Table 5.3 exhibit almost identical open voltages (V_{oc}); the short circuit currents (J_{sc}) of the solar cells on Ringo and Timepix chips are however smaller. This might be related to the high topography variation (i.e., step height) initially present on the chip's surface before post-processing. The Ringo chip has the highest topography variation, with 1.5 µm excursions. Insufficient step coverage of one of the solar cell layers will lead to increasing the cell's series resistance (R_s) or shunting the layers electrically i.e., decreasing the parallel resistance (R_p) and fill factor (FF). Indeed the solar cells on the Ringo chip exhibit both effects (See Table 5.3).

Table 5.5: Parameters of CIGS solar cells on Timepix chip at different peak substrate temperature.

Substrate T (ºC)	η	J_{sc} mA/cm2	V_{oc} V	FF	R_s Ω cm2	R_p Ω cm2
400	2.7%	16.8	0.44	0.37	13.6	79.5
425*	6.4%	21.48	0.48	0.61	4.2	289.5
450	7.1%	24.72	0.51	0.56	5.53	875.4

Table 5.5: Efficiency comparison of the PV cells on glass and on CMOS chip.

	Cell 1	Cell 2	Cell 3	Cell 4	average
Glass	6.8%	10.8%	10.0%	9.1%	9.2±1.7%
Cu-PCM	8.2%	8.6%	7.2%	9.2%	8.3±0.8%

The quality of the CIGS solar cell is related to the substrate temperature during the deposition [109, 204]. This is because a higher substrate temperature implies higher thermal energy available for a better activation of the layer-formation process. In the studied temperature range of 400-450 °C, this leads to a better crystal structure of the CIGS layer, as follows from the XRD results presented in Section 5.4.1. Fig. 5.12 confirms an improved solar cell behavior at the higher deposition temperatures.

5.4.3 Efficiency and yield

In the 2nd Run, several equal-size (22×22 mm^2) glass and Cu-PCM chips, which have a good Mo adhesion due to the use of 10-nm Ti adhesion layer, were mounted into the chip holder for the solar cell fabrication at 425 °C. The efficiencies of the solar cells on one glass plate and a Cu-PCM chip are listed in Table 5.4.

All efficiencies on this Cu-PCM chip from 2nd Run are higher than the best CIGS efficiency (7.1%) obtained without the Ti adhesion layer from the 1st Run, as reported in [146]. Further, the efficiency gap between the CMOS chip and the glass reference has decreased from 1~5% [146] to 0.9% in the new experiments.

If we consider < 4% efficiency threshold as the failure criterion, the yield on CMOS chips without Ti was generally less than 50% [146]. If proper adhesion is guaranteed by Ti layer, the yield on CMOS chip reaches 84%

(5 bad cells out of 32), which is comparable to that on glass substrate (88%, 4 bad cells out of 32).

5.4.4 Efficiency of PV cells versus chip topography

The efficiency of the solar cell is closely related to the surface profile amplitude and the Mo adhesion. Dedicated experiments were conducted to further investigate and quantify this phenomenon.

Fig. 5.13 shows a sketch of the additionally fabricated test samples (right image) used to investigate the influence of the substrate surface profile

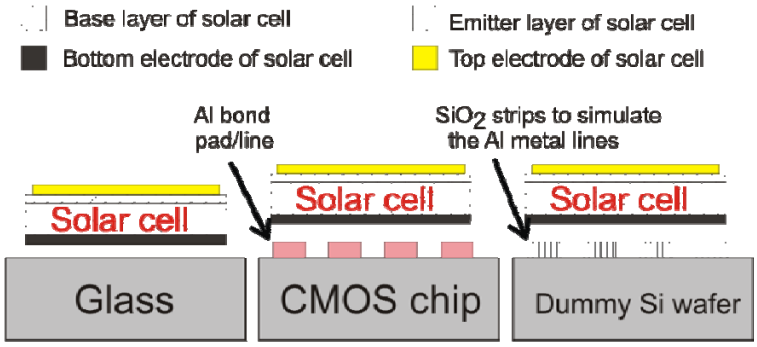

Fig. 5.14: Schematic diagram of substrates with different surface profile amplitude. Left: glass substrate; middle: standard CMOS chip with Al bond pads and lines embedded in the Si_3N_4 scratch protection layer; right: dedicated test samples with PECVD SiO_2 strips of different thickness (50~550 nm).

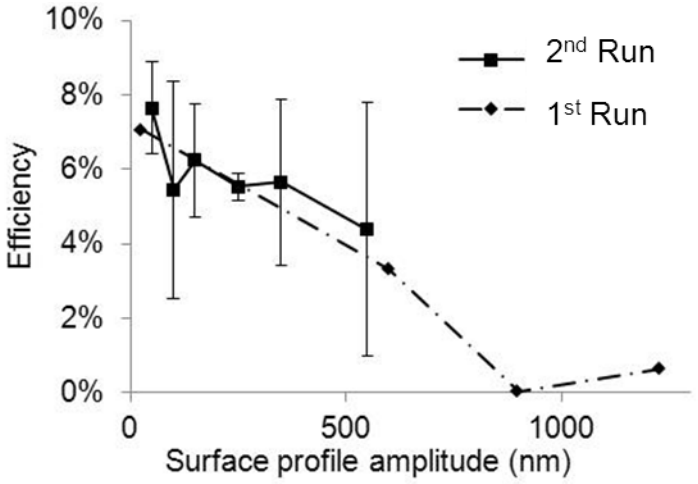

Fig. 5.14. Efficiency against surface profile amplitude. The 1st Run presented single measurements; hence no error bars were determined. All samples are fabricated at 425 ºC.

amplitude. PECVD SiO_2 stripes are used to mimic typical interconnect topography of CMOS chips. The width and spacing of the SiO_2 strips are 20 μm, giving an area coverage of ~50%. The thickness of the oxide varies from 50 nm to 550 nm. On each of the test samples, after Ti and Mo deposition, four CIGS solar cells are deposited.

Fig. 5.14 shows the averaged efficiency of the cells at different surface profile amplitude (i.e. the thickness of the SiO_2 stripes). A slight, gradual efficiency drop seems to occur with increasing topography, quantitatively in line with the earlier findings [146].

5.5 CMOS chip performance after the Solar cell Integration

In this section, the CMOS functionality after the CIGS solar cell integration will be addressed. We report on MOS capacitance-voltage and current-voltage characteristics; the behavior of ring oscillators; and the functionality of the mixed-signal Timepix microchips. In all cases, the same functionality tests are carried out before and after solar cell deposition and removal, and compared.

5.5.1 C-V and I-V measurements on Cu-PCM devices

The capacitance-voltage (*C-V*) curves of MOS capacitors and the current-voltage (*I-V*) curves of MOS transistors were measured using a Keithley 4200 semiconductor characterization system on Karl Suss PM8 low leakage probe station at the University of Twente. The Cu-PCM devices, with bond pads across the chip, had to be de-processed before electrical re-testing (see Section 5.3.3).

The MOS capacitor area was 1.44×10^{-6} cm^2 with an oxide thickness of 2.2 nm. The capacitance measurements were carried out at a frequency of 1 MHz. The MOSFET under study has a gate length of 130 nm. The transistor source and body were grounded, and gate and drain potentials varied for the transistor measurements.

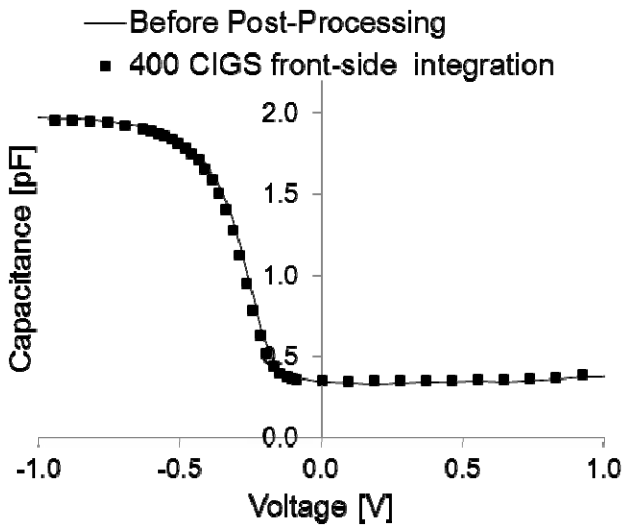

Fig. 5.16. *C-V* curves of a MOS capacitor before and after CIGS solar cell integration on chip's front-side at 400 ºC.

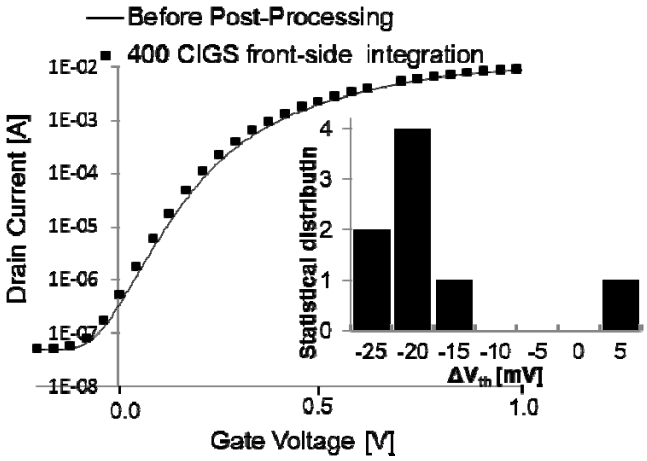

Fig. 5.16. *I-V* curves of a NMOS transistor before and after the same post-processing. The inset shows threshold voltage shift statistics of 8 transistors.

For an illustration, in Fig. 5.15 and Fig. 5.16, we present the *C-V* and *I-V* curves of the individual devices after 400 °C CIGS front-side integration. For all CIGS process conditions, the key device parameters studied are summarized in Table 5.6. It lists the changes in flatband voltage V_{FB}, threshold voltage V_{th}, and subthreshold swing *S*. Only small changes of the device

Table 5.6: Functional testing of MOS capacitors and MOSFETs on Cu-PCM chips after post- processing steps. The *Front* row stands for front-side integration of the cells; *Back* means backside integration. The last column shows the annealing experiment without the CIGS stack deposition.

Process Condition		400 ºC CIGS	425 ºC CIGS	450 ºC CIGS	450 ºC CIGS (No NaF)	450 ºC 30 min annealing
ΔV_{FB} (mV)	Front	-9	(no data)	-4	-4	-9
	Back	-6	-12	-10	-4	
ΔV_{th}(mV)	Front	-21	-39	-26	-26	-20
	Back	-21	-20	-25	-23	
ΔS (mV/dec)	Front	-1.4	-1.0	-1.3	-1.3	-1.2
	Back	-1.6	-1.4	-0.4	-1.3	

parameters are observed. They are most likely governed by the added thermal budget. This is supported by the control experiment where the chips were exposed to the same thermal budget but without the CIGS stack deposition: see the last column of Table 5.6.

An experiment, where the NaF deposition was skipped, meant to isolate a possible detrimental influence from Na contamination, yielded quite similar results as the others (Table 5.6 labeled "No NaF"). Quantitatively, the changes are comparable to packaging-related parameter shifts [151]. In summary, the 0.13-µm CMOS PCM chip does not show a significant influence of the solar cell integration to device parameters for both front- and back-side integrations.

5.5.2 Functionality of the Ringo chip

A ring oscillator (Ringo) is widely used as a tool to characterize the performance of MOSFETs [152]. In our experiments, the power consumption and the output frequency versus the enable voltage of the 17-stage ring oscillator have been measured before and after the solar cell integration by Keithley SCS 4200 and Agilent/HP 54642A oscilloscope. In this case, the solar cell was deliberately placed beside the ring oscillator test structure. Hence, no de-processing of the solar cell was required to do the final CMOS test. The results are shown in Fig. 5.17.

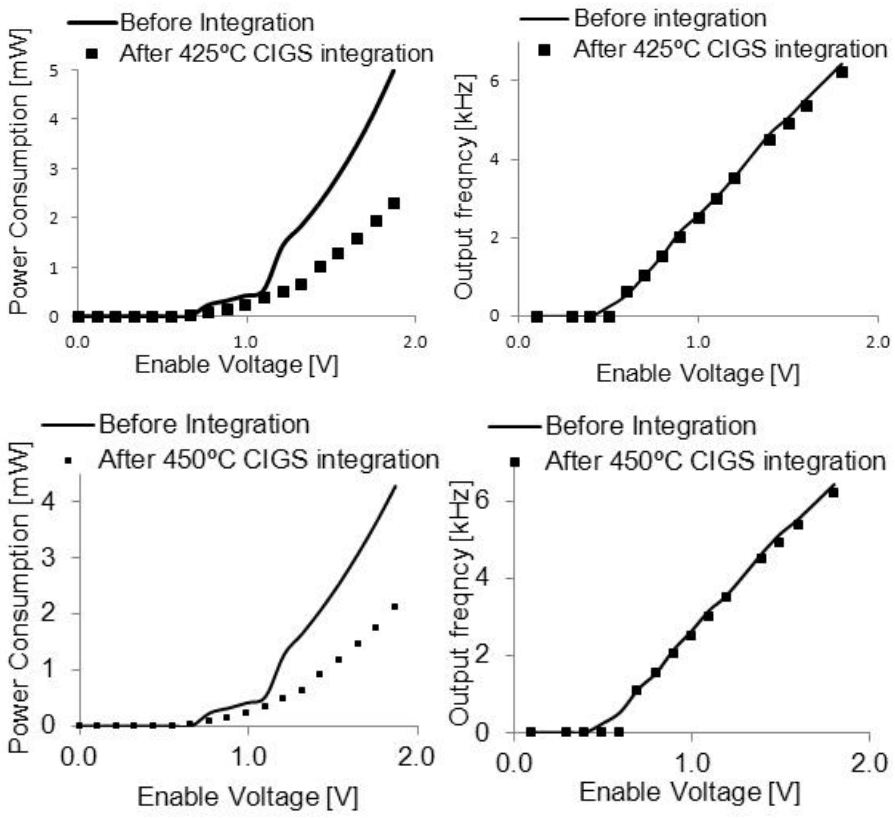

Fig. 5.17: Power consumption (left) and the output frequency (right) at different enable voltage of the ring oscillator before and after CIGS solar cell integration at 425 ºC (top) and 450 ºC (bottom) peak temperature. The ring oscillator is read out via an embedded 512-times frequency divider.

One can observe that there is little impact of the integration on the Ringo frequency. However, the power consumption does show a change after post-processing, likely due to threshold voltage shifts.

5.5.3 Functionality of Timepix chip

The detailed explanation of Timepix chip was presented in Section 3.1.3. As same as used in a-Si solar cells integration, the post-processed chips were of a lower-quality category as those normally used. A fraction of the pixels and columns therefore malfunctioned before solar cell integration.

Table 5.7: Functionality test results of Timepix chips after various post-processing sequences. (The process condition terminology is as in Table 5.6).

Process Condition		400 ºC CIGS	425 ºC CIGS	450 ºC CIGS	450 ºC CIGS (No NaF)	450 ºC 30 min anneal
Digital functional column	Front	254→228	malfunction	malfunction	malfunction	252→252
	Back	253→253	253→253	247→233	(no data)	
Analog functional Column	Front	254→212	malfunction	malfunction	malfunction	252→252
	Back	253→252	253→253	247→232	(no data)	

The Pixelman software [117] and an automated probe station were again employed for functional testing of the Timepix chips at the Nikhef Institute in Amsterdam (NL). A summary of the test results is presented in Table 5.7.

Values in the Table 5.7 give the number of columns (out of 256) passing the functionality test before and after post-processing. Good results are obtained with all backside-processed Timepix chips, with the front-side processed chip at 400 ºC, and with the reference experiment where the chip is only exposed to the additional thermal budget. Chips with backside-deposited CIGS (up to 425 ºC) maintain full IC functionality.

The chip functionality is however adversely influenced when CIGS solar cells are produced on the front side of the chip. The chip loses part of its functionality at 400 ºC, and malfunctions entirely at higher process temperatures. Some functionality loss is also observed on the 450 ºC backside-processed chips. It is concluded that the process window for front-side integration is very tight; the peak temperature should remain around or even below 400 ºC. For backside integration, the allowable peak temperature is about 50 ºC higher, and matches the required temperature for high-efficiency CIGS cells.

Compared with the results of the Cu-PCM chips, interconnect failure is a likely cause of the observed functionality loss. The combination of high temperature and mechanical stress may lead to metal line cracking; and Al interconnect (on Ringo and Timepix) is likely more vulnerable than Cu interconnect.

5.6 Conclusion

We conclude that CIGS thin-film solar cells can be integrated on CMOS microchips. CMOS functionality can be maintained both with Cu and with Al interconnect, as shown on chips from the 0.13-µm, 0.18-µm and 0.25-µm technology generations.

In case of strong topography of more than a few hundred nanometers, the CMOS IC should be planarized. It must be covered by a diffusion barrier, and possibly an adhesion layer; followed by the conventional PV process flow.

Considering the mechanical stress, a tight process window is found for the manufacturing of CIGS solar cells on the CMOS side of the microchip. If integrated on the front side, the process temperature should be kept around or below 400 ºC. At the present state of CIGS technology, this implies a loss in solar cell efficiency. But for backside integration, the process temperature can go up to 425 ºC.

If good adhesion between the Mo and passivated CMOS chip is provided, the solar cells on top show an efficiency of 8.4±0.8 % and a yield of 84%, both values close to the glass reference. The single-chip integration scheme shown in this work is suitable for wafer level processing.

Chapter 6. Conclusions and Recommendations

6.1 Conclusions

Energy harvesting is an interesting topic in the 21st century for electrical engineers from both industry and academia. It will be a core technology for autonomous wireless networks, which is the essential component of the long-lived ubiquitous computing world.

There are different ways to achieve the energy harvesting goal, and each of them has its own pros and cons. In this thesis, we focused on monolithic integration of an energy harvester on top of CMOS chips by CMOS compatible post-processing technologies, and two approaches have been studied.

Chapter 2 describes the first approach which is an integrated electromagnetic energy harvester, which aims to scavenging kinetic energy of the mechanical vibrations in the environment. The numerical simulations show that our EM energy harvester design can offer a power output at microwatts level, which is consistent with experimental results from other groups. However due to the absence of some required instruments and the frequency match challenge (page 28), the experimental realization was not carried out.

Chapter 3 to 5 describe the second approach which is integrated solar cells on top of CMOS chips without changing either the standard CMOS processing or the conventional solar cell technology. The integrated solar cells will harvest energy from light and transfer to the underneath CMOS circuits. After detailed consideration, a-Si solar cells and CIGS solar cells were chosen to be integrated on CMOS chips.

6.1.1 CMOS compatibility

The challenges for the solar cell integration are twofold: first, functional integrated solar cells on CMOS chip, second, the unaffected CMOS chip after the solar cell integration.

The possible damages were listed in Section 1.2.4, and we used three different CMOS chips to monitor the possible influence of the post-process (Section 3.1.3). A passivation layer should be first employed on both sides of the CMOS chip. Electrical characterizations have been done before and after the solar cell integration on Timepix (0.25 μm technology), Ring oscillator

(0.18 μm technology), and Cu-PCM (0.13μm technology) chips. These three different technology generations of CMOS chips can give generic information about the integration compatibility on three different levels, from a single device (MOS capacitor or MOSFET) via a single circuit (ring oscillator) to a complex CMOS chip (Timepix).

For a-silicon solar cells, the highest risk is the plasma charging damage, because for almost all the process steps of a-Si solar cell integration, plasma is involved which will be detrimental to the gate oxide of the transistors (gate oxides are sensitive to plasma charging damage). Thin silver layers are widely used to improve the a-Si solar cell efficiency, and this imposes silver metal ion contamination issues for CMOS circuits. The passivation layer stacks designed by us can avoid these two possible damages, which were confirmed by the CMOS chip performance comparison.

For CIGS solar cells, the highest risk to CMOS chips is the high process temperature. CIGS solar cells can be fabricated in a temperature range from 320 to 550 ºC, and for a higher PV efficiencies, we prefer a higher process temperature. However, a high fabrication temperature will damage the CMOS chips, because of the top Al metal lines of the CMOS chips will be damaged if the process temperature is higher than 450 ºC. In order to find highest allowed process temperature, experiment have been done for a relative safe temperature of 400 ºC, a relatively unsafe 450 ºC, and the middle one of 425 ºC. We found that the process temperature should be below 425 ºC.

The "low-k" oxide in the interconnect stack of the CMOS chip is brittle, and could not support high mechanical stress, so the added CIGS solar cell layers can mechanically damage the underlying CMOS circuits. This stress is also related to the temperature: the higher the temperature, the higher the stress. We found that for the same process temperature of 425 ºC, the backside integration is CMOS compatible, while front-side integration will influence the performance of the CMOS chip. And this is due to the mechanical stress of the added solar cell layers.

As to the Na^+ contamination, our passivation layers can prevent the CMOS chip from the Na^+, which is again confirmed by the CMOS chip performance comparison.

In short, as for CIGS solar cells, to maintain the functionality of the CMOS chips, the integration was preferred to be done on the backside and at a temperature below 425 °C.

6.1.2 PV efficiency and yield on CMOS chips

We want PV cells integrated CMOS chips have similar efficiency and yield as that on sola lime glass substrate normally used in solar cell industry and research. There are two challenges for this: the surface profile amplitude and adhesion between the CMOS chip and the solar cell.

Conventional soda lime glass substrates have a surface profile amplitude less than 50 nm. A CMOS chip's surface profile amplitude may vary from several hundred nanometers to more than 1500 nm depending on the final pattering step of the CMOS chip. Soda lime glass is composed of amorphous SiO_2, the top surface of the CMOS chips before solar cell integration is PECVD SiO_2.

Our experiments have shown that the surface profile on CMOS chips will negatively influence the yield of the a-Si solar cell and the PV efficiency of the CIGS solar cells. The conventional CIGS process steps, which can guarantee a good adhesion of solar cells on glass substrates, could not have a good adhesion on CMOS chips.

The technological solutions, proposed in this work, allow us to improve the yield and the efficiency of the solar cells on CMOS chips. By applying 3 μm of BCB planarizing layer before the a-Si solar cells integration, the solar cells on-chip showed an efficiency around 7.1% and a yield of 92%. The CIGS solar cells on CMOS demonstrated an efficiency of 8.4 % and a yield of 84%, provided that a good Mo adhesion is achieved by a 10-nm-thick Ti adhesion layer. For both types of the solar cells, the efficiency and the yield are close to those of the glass-reference sample.

When using solar cells as energy harvesters, more than 7 mW/cm^2 can be supplied to the underlying CMOS circuits under AM1.5 illumination; for indoor light, the power output density can reach 0.6~6 $\mu W/cm^2$, depending on the distance between the light source and the harvester and the indoor light intensity.

Summarizing, in this thesis, two approaches to CMOS compatible integration of solar cells as energy harvesters are successfully demonstrated.

6.1.3 Comparison of technologies

In this thesis, three types of devices have been discussed, and they are EM energy harvester based on mechanical vibration, integrated a-Si solar cells energy harvester, and integrated CIGS solar cell energy harvester.

The frequency match challenge could not rule out vibration-based energy harvesters completely. In some cases, the available energy sources are limited to mechanical vibration energy sources; in other cases, the mechanical vibration sources have a stable fixed frequency, the vibration-based energy harvester is still preferred.

We studied the integration of a-Si solar cells and CIGS solar cells as energy harvesters on top of CMOS chips. The a-Si solar integration shows better CMOS compatibility, while the integrated CIGS solar cells show a higher efficiency (under AM 1.5 illumination). However, under weak light illuminations, especially the illumination intensity is below 1 mW/cm^2, a-Si solar cells maybe have a higher efficiency than the CIGS solar cells[1].

In three cases, CIGS solar cells integration may be a competitive candidate. First, the interconnections and the metal lines of the CMOS chips are all made of Cu, i.e., eliminating the use of Al. Such CMOS chips can tolerate high process temperature, then the CMOS compatibility may be kept even the CIGS solar cell integration is done at 500 ºC, which will lead to a high PV efficiency (>15%). Of course, the CMOS compatibility of the integration on such all-Cu-backend CMOS chips needs experimental testing by a similar procedure as shown in this thesis.

Second, the energy harvester will be used in outdoor illuminations such as in sunlight. Even if CIGS is fabricated with a process temperature limited to 400 ºC, the efficiency CIGS solar cells can easily surpass the best efficiency (10%) from a-Si solar cells.

[1] At least according the literatures available now [23, 24, 105].

Finally, the harvester will be used in an environment where high radiations are present, for example, in outer space. CIGS solar cells have an exceptionally good radiation hardness and stability which outperforms a-Si solar cells.

Except the aforementioned situations, a-Si solar cell technology is a preferred choice for integration on CMOS chips. Another reason behind this is that, a-Si solar cells mainly use silicon, which is a familiar material for IC industry. In other words, this is in line with the guiding rule: *if it can be made of silicon, then make it of silicon.*

6.2 Recommendation

This thesis only provides the preliminary results of solar cells integration on CMOS chips for energy harvesting. To further study the feasibility of direct on-CMOS integration, the following aspects need to be additionally investigated:

1) The electrical connection between the solar cell and the CMOS circuit should be realized. For a front-side solar cell integration, vertical metal vias through the passivation layer can be realized; for a back-side integration, through-silicon-vias can be a solution.
2) Testing the solar cell efficiency under "indoor light" illuminations. We suggest the following measurements[1]. First, we can measure the efficiency at a reduced-intensity AM 1.5 spectrum, i.e., by applying the neutral density filters and obtaining the solar cell parameters from 100% down to 0.1% of the illumination. In this case, the light spectrum corresponds to that of AM 1.5 illumination, only the intensity is reduced. Second, we can illuminate the cells with a given (known) fluorescent light, and to extract the efficiency value. This needs a calibrated light spectrum as the reference.
3) Matching the output voltage of solar cells and the input voltage of CMOS chips. The maximum output voltages are 0.4 V and 0.7 V for CIGS and a-Si solar cells, respectively. For CMOS circuits, the supply voltage is normally larger than 1 V, so the output voltage of the solar cells needs to be increased. This can be solved, on one hand, by con-

[1] Personal communication with Prof. Schropp in March, 2011

necting two a-Si or four CIGS solar cells in series, with the corresponding lithography and etch steps. On the other hand, multi-junction or tandem solar cells (both having an output voltage > 1.5 volts) can be realized. This leads to additional technological challenges during the solar cell integration.

4) For a complete "harvester-on-chip" system, power-management circuits and energy buffers need to be realized. Because of the low output energy, a proper management of the scavenged energy and an efficient energy buffer are required. The power management circuit should be a part of the CMOS IC chip, and the buffer can be a supercapacitor.
5) More investigations on a higher efficiency under indoor light illumination. The solar cell technologies nowadays are optimized for higher efficiency under AM 1.5 spectrum, which simulates the outdoor sunlight. Little has been done for better solar cell efficiency under indoor light illumination conditions. Maybe this is due to the lack of an international standard indoor spectrum, so the beginning of the improvement may be an international indoor light spectrum. After that, technically there are two possible ways to have a better indoor light PV cell. First and the most important, tuning the bandgap of the solar cell material, so that it will match the indoor light spectrum. For a-Si solar cells, this can be achieved by varying the hydrogen content inside the Si layers, for CIGS this can be achieved by varying the amount of Ga. Secondly, improving the quality of the emitter layer of the solar cell layer. The indoor light have a low light intensity and a higher energy, so most of it will be absorbed inside the first several hundred nanometers of the functional layer, which is basically the emitter layer of the solar cell.
6) Last but not at least, the integration of solar cells on a CMOS chip which contains a wireless sensor node as well as powering the wireless sensor node by the above-integrated solar cells at different illumination conditions.

Reference

[1] ITU, "Ubiquitous Network society," http://www.itu.int/WORLD2006/forum/ubiquitous_network_society.html.

[2] M. Weiser, "The Computer for the Twenty-First Century," *Scientific American,* vol. 265, no. 3, pp. 94-104, 1991.

[3] M. Weiser, "Some computer science issues in ubiquitous computing," *Commun. ACM,* vol. 36, no. 7, pp. 75-84, 1993.

[4] B. Warneke, M. Last, B. Liebowitz *et al.*, "Smart dust: communicating with a cubic-millimeter computer," *Computer,* vol. 34, no. 1, pp. 44-51, 2001.

[5] V. Pop, H. J. Bergveld, P. H. L. Notten *et al.*, "State-of-the-art of battery state-of-charge determination," *Measurement Science and Technology,* vol. 16, no. 12, 2005.

[6] R. Huggins, Advanced batteries : materials science aspects, Berlin: Springer, 2009.

[7] J. M. Tarascon, "Key challenges in future Li-battery research," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences,* vol. 368, no. 1923, pp. 3227-3241, 2010.

[8] J. A. Paradiso, and T. Starner, "Energy scavenging for mobile and wireless electronics," *IEEE Pervasive Computing,* vol. 4, no. 1, pp. 18-27, 2005.

[9] M. Armand, and J. M. Tarascon, "Building better batteries," *Nature,* vol. 451, no. 7179, pp. 652-657, 2008.

[10] S. K. Chou, W. M. Yang, K. J. Chua *et al.*, "Development of micro power generators - A review," *Applied Energy,* vol. 88, no. 1, pp. 1-16, 2011.

[11] A. Kundu, J. H. Jang, J. H. Gil *et al.*, "Micro-fuel cells-Current development and applications," *Journal of Power Sources,* vol. 170, no. 1, pp. 67-78, 2007.

[12] A. Evans, A. Bieberle-Hütter, J. L. M. Rupp *et al.*, "Review on microfabricated micro-solid oxide fuel cell membranes," *Journal of Power Sources,* vol. 194, no. 1, pp. 119-129, 2009.

[13] R. Amirtharajah, and A. P. Chandrakasan, "Self-powered signal processing using vibration-based power generation," *IEEE Journal of Solid-State Circuits,* vol. 33, no. 5, pp. 687-695, 1998.

[14] S. Hanson, Z. Foo, D. Blaauw *et al.*, "A 0.5 V sub-microwatt CMOS image sensor with pulse-width modulation read-out," *IEEE Journal of Solid-State Circuits,* vol. 45, no. 4, pp. 759-767, 2009.

[15] A. C. Paglinawan, Y. H. Wang, S. C. Cheng *et al.*, "CMOS temperature sensor with constant power consumption multi-level comparator for implantable bio-medical devices," *Electronics Letters,* vol. 45, no. 25, pp. 1291-1292, 2009.

[16] S. Roundy, P. K. Wright, and J. Rabaey, "A study of low level vibrations as a power source for wireless sensor nodes," *Computer Communications,* vol. 26, no. 11, pp. 1131-1144, 2003.

[17] S. Roundy, P. K. Wright, and J. M. Rabaey, *Energy scavenging for wireless sensor networks : with special focus on vibrations*, Boston: Kluwer Academic Publishers, 2004.

[18] G. E. Moore, "Gramming more components onto integrated circuits," *Electronics,* vol. 38, no. 8, pp. 114-117, 1965.

[19] J. Schmitz, "Adding functionality to microchips by wafer post-processing," Nuclear Instruments and Methods in Physics Research A, vol. 576, no. 1, pp. 142-149, 2007.

[20] "Reference Solar Spectral Irradiance: Air Mass 1.5," http://rredc.nrel.gov/solar/spectra/am1.5/#about.

[21] M. D. Archer, and R. Hill, *Clean electricity from photovoltaics*, London: Imperial College Press, 2001.

[22] M. A. Green, K. Emery, Y. Hishikawa *et al.*, "Solar cell efficiency tables (version 37)," *Progress in Photovoltaics: Research and Applications,* vol. 19, no. 1, pp. 84-92, 2011.

[23] J. F. Randall, and J. Jacot, "Is AM1.5 applicable in practice? Modelling eight photovoltaic materials with respect to light intensity and two spectra," *Renewable Energy,* vol. 28, no. 12, pp. 1851-1864, 2003.

H[24]N.H. Reich, W.G.J.H.M. van Sark, E.A. Alsema, S. Silvester, A.S.H. van der Heide, R.W. Lof and R.E.I. Schropp, "Weak light performance and spectral response of different solar cell types," in 20th European Photovoltaic Solar Energy Conference and Exhibition, Barcelona, Spain 2005.

[25] S. Teske, T. Pregger, S. Simon *et al.*, "Energy [R]evolution 2010-a sustainable world energy outlook," *Energy Efficiency*, pp. 1-25, 2010.

[26] C. C. Federspiel, and J. Chen, "Air-Powered Sensor," *Second International Conference on Sensors: IEEE Sensors 2003.* pp. 22-25.

[27] D. Rancourt, A. Tabesh, and L. G. Fréchette, "Evaluation of centimeter-scale micro wind mills: Aerodynamics and electromagnetic power generation ". pp. 93-96, Proceedings of PowerMEMS 2007, Nov 28 - 29, Freiburg, Germany.

[28] R. Myers, M. Vickers, H. Kim *et al.*, "Small scale windmill," *Applied Physics Letters,* vol. 90, no. 5, 2007.

[29] A. S. Holmes, G. Hong, K. R. Pullen *et al.*, "Axial-flow microturbine with electromagnetic generator: Design, cfd simulation, and prototype demonstration," *17th IEEE International Conference on Micro Electro Mechanical Systems (MEMS): Maastricht MEMS 2004 Technical Digest.* pp. 568-571.

[30] P. B. S. Lissaman, "Low-Reynolds-Number Airfoils," *Annual Review of Fluid Mechanics,* vol. 15, pp. 223-239, 1983.

[31] G. J. Snyder, and T. S. Ursell, "Thermoelectric efficiency and compatibility," *Physical Review Letters,* vol. 91, no. 14, 2003.

[32] W. Seifert, K. Zabrocki, E. Müller *et al.*, "Power-related compatibility and maximum electrical power output of a thermogenerator," *Physica Status Solidi (A) Applications and Materials,* vol. 207, no. 10, pp. 2399-2406, 2010.

[33] P. D. Mitcheson, "Energy harvesting for human wearable and implantable bio-sensors," 2010 32nd Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBC'10. pp. 3432-3436.

[34] S. M. Yang, T. Lee, and C. A. Jeng, "Development of a thermoelectric energy harvester with thermal isolation cavity by standard CMOS process," *Sensors and Actuators, A: Physical,* vol. 153, no. 2, pp. 244-250, 2009.

[35] R. Venkatasubramanian, C. Watkins, D. Stokes *et al.*, "Energy harvesting for electronics with thermoelectric devices using nanoscale materials," *2007 IEEE International Electron Devices Meeting,* pp. 367-370.

[36] M. Strasser, R. Aigner, C. Lauterbach *et al.*, "Micromachined CMOS thermoelectric generators as on-chip power supply," *Sensors and Actuators, A: Physical,* vol. 114, no. 2-3, pp. 362-370, 2004.

[37] H. Böttner, J. Nurnus, A. Gavrikov *et al.*, "New thermoelectric components using microsystems technologies," *Journal of Microelectromechanical Systems,* vol. 13, no. 3, pp. 414-420, 2004.

[38] T. Starner, and J. Paradiso, "Human Generated Power for Mobile Electronics," In: C. Piguet, Editor, Low power electronics design, CRS Press (2004), www-static.cc.gatech.edu.

[39] N. S. Shenck, and J. A. Paradiso, "Energy scavenging with shoe-mounted piezoelectrics," *IEEE Micro,* vol. 21, no. 3, pp. 30-42, 2001.

[40] A. D. Kuo, "Harvesting energy by improving the economy of human walking," *Science,* vol. 309, no. 5741, pp. 1686-1687, 2005.

[41] J. F. Antaki, G. E. Bertocci, E. C. Green *et al.*, "A gait-powered autologous battery charging system for artificial organs," *ASAIO Journal,* vol. 41, no. 3, 1995.

[42] T. Von Büren, P. D. Mitcheson, T. C. Green *et al.*, "Optimization of inertial micropower generators for human walking motion," *IEEE Sensors Journal,* vol. 6, no. 1, pp. 28-37, 2006.

[43] P. D. Mitcheson, E. M. Yeatman, G. K. Rao *et al.*, "Energy harvesting from human and machine motion for wireless electronic devices," *Proceedings of the IEEE,* vol. 96, no. 9, pp. 1457-1486, 2008.

[44] J. D. Jackson, *Classical Electrodynamics*, pp. 562, Hoboken, NJ: John Wiley & Sons, 1998.

[45] D. Friedman, H. Heinrich, and D. W. Duan, "Low-power CMOS integrated circuit for field-powered radio frequency identification tags," *Proceedings of the 1997 IEEE International Solid-State Circuits Conference, ISSCC.* pp. 294-295.

[46] A. Ahlbom, U. Bergqvist, J. H. Bernhardt *et al.*, "Guidelines for limiting exposure to time-varying electric, magnetic, and electromagnetic fields (up to 300 GHz)," *Health Physics,* vol. 74, no. 4, pp. 494-521, 1998.

[47] IEEE. committee, "IEEE Standard for Safety Levels With Respect to Human Exposure to Radio Frequency Electromagnetic Fields, 3 kHz to 300 GHz," *IEEE Std C95.1-2005 (Revision of IEEE Std C95.1-1991)*, 2006.

[48] L. Anglesio, A. Benedetto, A. Bonino *et al.*, "Population exposure to electromagnetic fields generated by radio base stations: Evaluation of the urban background by using provisional model and instrumental measurements," *Radiation Protection Dosimetry,* vol. 97, no. 4, pp. 355-358, 2001.

[49] J. B. Burch, M. Clark, M. G. Yost *et al.*, "Radio frequency nonionizing radiation in a community exposed to radio and television broadcasting," *Environmental Health Perspectives,* vol. 114, no. 2, pp. 248-253, 2006.

[50] U. Kaiser, and W. Steinhagen, "Low-power transponder IC for high-performance identification systems," *IEEE Journal of Solid-State Circuits,* vol. 30, no. 3, pp. 306-310, 1995.

[51] A. Shameli, A. Safarian, A. Rofougaran *et al.*, "Power harvester design for passive UHF RFID tag using a voltage boosting technique," *IEEE Transactions on Microwave Theory and Techniques,* vol. 55, no. 6, pp. 1089-1096, 2007.

[52] J. A. Hagerty, F. B. Helmbrecht, W. H. McCalpin *et al.*, "Recycling ambient microwave energy with broad-band rectenna arrays," *IEEE Transactions on Microwave Theory and Techniques,* vol. 52, no. 3, pp. 1014-1024, 2004.

[53] M. H. Mickle, M. Mi, L. Mats *et al.*, "Powering autonomous cubic-millimeter devices," *IEEE Antennas and Propagation Magazine,* vol. 48, no. 1, pp. 11-21, 2006.

[54] S. P. Beeby, M. J. Tudor, and N. M. White, "Energy harvesting vibration sources for microsystems applications," *Measurement Science and Technology,* vol. 17, no. 12, 2006.

[55] Y. Li, Z. Cheng, H. San *et al.*, "Design and simulation of a capacitive vibration energy generator based on radioisotope ^{63}Ni," *5th IEEE International Conference on Nano/Micro Engineered and Molecular Systems, NEMS 2010.* pp. 78-83.

[56] H. Li, A. Lal, J. Blanchard *et al.*, "Self-reciprocating radioisotope-powered cantilever," *Journal of Applied Physics,* vol. 92, no. 2, pp. 1122, 2002.

[57] S. Roundy, D. Steingart, L. Frechette *et al.*, "Power sources for wireless sensor networks," Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 2004, pp. 1-17.

[58] R. J. M. Vullers, R. V. Schaijk, H. J. Visser *et al.*, "Energy Harvesting for Autonomous Wireless Sensor Networks," *Solid-State Circuits Magazine, IEEE,* vol. 2, no. 2, pp. 29-38, 2010.

[59] M. K. van Veen, and R. E. I. Schropp, "Amorphous silicon deposited by hot-wire CVD for application in dual junction solar cells," *Thin Solid Films,* vol. 403-404, pp. 135-138, 2002.

[60] R. Elfrink, V. Pop, D. Hohlfeld *et al.*, "First autonomous wireless sensor node powered by a vacuum-packaged piezoelectric MEMS energy harvester," *2009 International Electron Devices Meeting,* pp. 22.5.1-22.5.4 2009.

[61] P. Glynne-Jones, M. J. Tudor, S. P. Beeby *et al.*, “An electromagnetic, vibration-powered generator for intelligent sensor systems,” *Sensors and Actuators, A: Physical,* vol. 110, no. 1-3, pp. 344-349, 2004.

[62] T. Tsutsummo, Y. Suzuki, N. Kasagi *et al.*, "Seismic power generator using high-performance polymer electret," *19th IEEE International Conference on Micro Electro Mechanical Systems.* pp. 98-101, 2006.

[63] C. B. Williams, and R. B. Yates, “Analysis of a micro-electric generator for microsystems,” *Sensors and Actuators, A: Physical,* vol. 52, no. 1-3, pp. 8-11, 1996.

[64] N. N. H. Ching, H. Y. Wong, W. J. Li *et al.*, “A laser-micromachined multi-modal resonating power transducer for wireless sensing systems,” *Sensors and Actuators, A: Physical,* vol. 97-98, pp. 685-690, 2002.

[65] S. P. Beeby, R. N. Torah, M. J. Tudor *et al.*, “A micro electromagnetic generator for vibration energy harvesting,” *Journal of Micromechanics and Microengineering,* vol. 17, no. 7, pp. 1257-1265, 2007.

[66] E. Bouendeu, A. Greiner, P. J. Smith *et al.*, “A low-cost electromagnetic generator for vibration energy harvesting,” *IEEE Sensors Journal,* vol. 11, no. 1, pp. 107-113, 2011.

[67] H. Raisigel, O. Cugat, and J. Delamare, “Permanent magnet planar micro-generators,” *Sensors and Actuators, A: Physical,* vol. 130-131, no. SPEC. ISS., pp. 438-444, 2006.

[68] O. Cugat, J. Delamare, and G. Reyne, “Magnetic Micro-Actuators and Systems (MAGMAS),” *IEEE Transactions on Magnetics,* vol. 39, no. 6, pp. 3607-3612, 2003.

[69] S. Meninger, J. O. Mur-Miranda, R. Amirtharajah *et al.*, “Vibration-to-electric energy conversion,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 9, no. 1, pp. 64-76, 2001.

[70] Y. Chiu, C.-T. Kuo, and Y.-S. Chu, “MEMS design and fabrication of an electrostatic vibration-to-electricity energy converter,” *Microsystem Technologies,* vol. 13, no. 11, pp. 1663-1669, 2007.

[71] P. Miao, P. D. Mitcheson, A. S. Holmes *et al.*, “Mems inertial power generators for biomedical applications,” *Microsystem Technologies,* vol. 12, no. 10-11, pp. 1079-1083, 2006.

[72] T. Sterken, P. Fiorini, G. Altena *et al.*, "Harvesting energy from vibrations byamicromachined electret generator," *4th International Conference on Solid-State Sensors, Actuators and Microsystems, TRANSDUCERS and EUROSENSORS '07.* pp. 129-132.

[73] S. Roundy, and P. K. Wright, “A piezoelectric vibration based generator for wireless electronics,” *Smart Materials and Structures,* vol. 13, no. 5, pp. 1131-1142, 2004.

[74] S. R. Anton, and H. A. Sodano, “A review of power harvesting using piezoelectric materials (2003-2006),” *Smart Materials and Structures,* vol. 16, no. 3, 2007.

[75] N. S. Hudak, and G. G. Amatucci, “Small-scale energy harvesting through thermoelectric, vibration, and radiofrequency power conversion,” *Journal of Applied Physics,* vol. 103, no. 10, 2008.

[76] P. L. Cavallotti, N. Lecis, H. Fauser *et al.*, "Electrodeposition of magnetic multilayers," *Surface and Coatings Technology,* vol. 105, no. 3, pp. 232-239, 1998.

[77] F. M. F. Rhen, E. Backen, and J. M. D. Coey, "Thick-film permanent magnets by membrane electrodeposition," *Journal of Applied Physics,* vol. 97, no. 11, pp. 1-4, 2005.

[78] COMSOL. http://www.comsol.nl/.

[79] Visimag, "Visualizing Magnetic Fields," http://www.vizimag.com/.

[80] J. Jackson, Classical Electrodynamics Third Edition: Wiley, pp 354,1998.

[81] M. Sagawa, S. Fujimura, S. Yamamoto *et al.*, "Permanent magnet materials based on the rare earth-iron-boron tetragonal compounds," *1984 International Magnetics Conference (INTERMAG).* pp. 1584-1589.

[82] B. A. Kapitanov, N. V. Kornilov, Y. L. Linetsky *et al.*, "Sputtered permanent Nd-Fe-B magnets," *Journal of Magnetism and Magnetic Materials,* vol. 127, no. 3, pp. 289-297, 1993.

[83] E. E. Aktakka, R. L. Peterson, and K. Najafi, "A CMOS-Compatible Piezoelectric Vibration Energy Scavenger Based on the Integration of Bulk PZT Films on Silicon," *2010 International Electron Devices Meeting,* pp. 31.5.1-31.5.4, 2010.

[84] S. Roundy, and Y. Zhang, "Toward self-tuning adaptive vibration based micro-generators," *Smart Structures, Devices, and Systems II.* pp. 373-384, 2005.

[85] D. S. Nguyen, E. Halvorsen, G. U. Jensen *et al.*, "Fabrication and characterization of a wideband MEMS energy harvester utilizing nonlinear springs," *Journal of Micromechanics and Microengineering,* vol. 20, no. 12, art. no. 125009, 2010.

[86] Ö. Zorlu, E. T. Topal, and H. Külah, "A vibration-based electromagnetic energy harvester using mechanical frequency up-conversion method," *IEEE Sensors Journal,* vol. 11, no. 2, pp. 481-488, 2011.

[87] B. Yang, C. Lee, W. Xiang *et al.*, "Electromagnetic energy harvesting from vibrations of multiple frequencies," *Journal of Micromechanics and Microengineering,* vol. 19, no. 3, art. no. 035001 , 2009.

[88] V. R. Challa, M. G. Prasad, Y. Shi *et al.*, "A vibration energy harvesting device with bidirectional resonance frequency tunability," *Smart Materials and Structures,* vol. 17, no. 1, art. no. 015035, 2008.

[89] A. J. Mouthaan, "Integrated cascade of photovoltaic cells as a power supply for integrated circuits," *Sensors and Actuators,* vol. 5, no. 4, pp. 285-292, 1984.

[90] O. Bulteel, R. Delamare, and D. Flandre, "High-efficiency solar cell embedded in SOI substrate for ULP autonomous circuits," *2009 IEEE International SOI Conference*.

[91] R. E. I. Schropp, and M. Zeman, Amorphous and microcrystalline silicon solar cells : modeling, materials, and device technology, Boston: Kluwer Academic, 1998.

[92] Wikipedia, "Timeline of solar cells,"

http://en.wikipedia.org/wiki/Timeline_of_solar_cells#cite_note-2.

[93] D. M. Chapin, C. S. Fuller, and G. L. Pearson, "A new silicon p-n junction photocell for converting solar radiation into electrical power," *Journal of Applied Physics,* vol. 25, no. 5, pp. 676-677, 1954.

[94] T. M. Razykov, C. S. Ferekides, D. Morel, E. Stefanakos, H. S. Ullal, and H. M. Upadhyaya, "Solar photovoltaic electricity: Current status and future prospects," *Solar Energy*, 2011.

[95] A. Shah, P. Torres, R. Tscharner *et al.*, "Photovoltaic technology: The case for thin-film solar cells," *Science,* vol. 285, no. 5428, pp. 692-698, 1999.

[96] S. M. Sze, and K. K. Ng, *Physics of semiconductor devices*, pp. 23, 213, Hoboken, NJ: Wiley-Interscience, 2007.

[97] R. J. Komp, Practical photovoltaics : electricity from solar cells, Ann Arbor, Mich.: Aatec, 2002.

[98] M. A. Green, "Third generation photovoltaics advanced solar energy conversion," http://dx.doi.org/10.1007/b137807.

[99] A. Shah, *Thin-film silicon solar cells*, Lausanne; Boca Raton: EPFL Press ; distributed by CRC Press, 2010.

[100] M. B. Prince, "Silicon solar energy converters," *Journal of Applied Physics,* vol. 26, no. 5, pp. 534-540, 1955.

[101] R. Hulstrom, R. Bird, and C. Riordan, "Spectral solar irradiance data sets for selected terrestrial conditions," *Solar Cells,* vol. 15, no. 4, pp. 365-391, 1985.

[102] A. Nasiri, S. A. Zabalawi, and G. Mandic, "Indoor power harvesting using photovoltaic cells for low-power applications," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 11, pp. 4502-4509, 2009.

[103] A. Hande, T. Polk, W. Walker *et al.*, "Indoor solar energy harvesting for sensor network router nodes," *Microprocessors and Microsystems,* vol. 31, no. 6, pp. 420-432, 2007.

[104] H. Shao, C. Y. Tsui, and W. H. Ki, "The design of a micro power management system for applications using photovoltaic cells with the maximum output power control," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 17, no. 8, pp. 1138-1142, 2009.

H[105] A. Virtuani, E. Lotter, and M. Powalla, "Performance of Cu(In,Ga)Se_2 solar cells under low irradiance," *Thin Solid Films,* vol. 431-432, pp. 443-447, 2003.

[106] Y. Li, K. S. Moon, and C. P. Wong, "Electronics without lead," *Science,* vol. 308, no. 5727, pp. 1419-1420, 2005.

[107] A. Hinsch, J. M. Kroon, R. Kern *et al.*, "Long-term stability of dye-sensitised solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 9, no. 6, pp. 425-438, 2001.

[108] M. Jørgensen, K. Norrman, and F. C. Krebs, "Stability/degradation of polymer solar cells," *Solar Energy Materials and Solar Cells,* vol. 92, no. 7, pp. 686-714, 2008.

[109] W. N. Shafarman, and J. Zhu, "Effect of substrate temperature and deposition profile on evaporated Cu(InGa)Se_2 films and devices," *Thin Solid Films,* vol. 361, pp. 473-477, 2000.

[110] X. Llopart, R. Ballabriga, M. Campbell *et al.*, "Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements," *Nuclear Instruments and Methods in Physics Research A,* vol. 581, no. 1-2 SPEC. ISS., pp. 485-494, 2007.

[111] V. M. Blanco Carballo, M. Chefdeville, M. Fransen *et al.*, "A radiation imaging detector made by postprocessing a standard CMOS chip," *IEEE Electron Device Letters,* vol. 29, no. 6, pp. 585-587, 2008.

[112] J. Melai, A. Breskin, M. Cortesi et al., "A UV sensitive integrated Micromegas with Timepix readout," Nuclear Instruments and Methods in Physics Research, vol. 628, no. 1, pp. 133-137, 2011.

[113]"MESA+ cleanroom for nanotechnology," http://www.utwente.nl/mesaplus/nanolab/.

[114] K. R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing-Part II," *Microelectromechanical Systems, Journal of,* vol. 12, no. 6, pp. 761-778, 2003.

[115] Oxford Instruments, http://www.oxford-instruments.com/Pages/home.aspx.

[116] Keithley, "Model 4200-SCS Reference Manual," http://www.keithley.com/.

[117] T. Holy, J. Jakubek, S. Pospisil et al., "Data acquisition and processing software package for Medipix2," Nuclear Instruments and Methods in Physics Research A, vol. 563, no. 1, pp. 254-258, 2006.

[118] H. F. Sterling, and R. C. G. Swann, "Chemical vapour deposition promoted by r.f. discharge," *Solid State Electronics,* vol. 8, no. 8, pp. 653-654, 1965.

[119] R. C. Chittick, J. H. Alexander, and H. F. Sterling, "Preparation and properties of amorphous silicon," *Electrochem Soc-J,* vol. 116, no. 1, pp. 77-81, 1969.

[120] W. E. Spear, and P. G. Le Comber, "Substitutional doping of amorphous silicon," *Solid State Communications,* vol. 17, no. 9, pp. 1193-1196, 1975.

[121] W. E. Spear, and P. G. Le Comber, "Electronic properties of substitutionally doped amorphous Si and Ge," *Philos Mag,* vol. 33, no. 6, pp. 935-949, 1976.

[122] D. E. Carlson, and C. R. Wronski, "Amorphous silicon solar cell," *Applied Physics Letters,* vol. 28, no. 11, pp. 671-673, 1976.

[123] M. K. Van Veen, C. H. M. Van Der Werf, and R. E. I. Schropp, "Tandem solar cells deposited using hot-wire chemical vapor deposition," *Journal of Non-Crystalline Solids,* vol. 338-340, no. 1 SPEC. ISS., pp. 655-658, 2004.

[124] J. Meier, P. Torres, R. Platz *et al.*, "On the way towards high efficiency thin film silicon solar cells by the 'micromorph' concept," *Proceedings of the 1996 MRS Spring Symposium.* pp. 3-14, 1996.

[125] R. E. I. Schropp, H. Li, R. H. J. Franken *et al.*, "Nanostructured thin films for multibandgap silicon triple junction solar cells," *Solar Energy Materials and Solar Cells,* vol. 93, no. 6-7, pp. 1129-1133, 2009.

[126] J. Yang, A. Banerjee, and S. Guha, "Triple-junction amorphous silicon alloy solar cell with 14.6% initial and 13.0% stable conversion efficiencies," *Applied Physics Letters,* vol. 70, no. 22, pp. 2975-2977, 1997.

[127] Y. Hattori, D. Kruangam, T. Toyama *et al.*, "Highly conductive p-type microcrystalline SiC:H prepared by ECR plasma CVD," *Applied Surface Science,* vol. 33-34, no. C, pp. 1276-1284, 1988.

[128] A. V. Shah, H. Schade, M. Vanecek *et al.*, "Thin-film silicon solar cell technology," *Progress in Photovoltaics: Research and Applications,* vol. 12, no. 2-3, pp. 113-142, 2004.

[129] J. Müller, B. Rech, J. Springer *et al.*, "TCO and light trapping in silicon thin film solar cells," *Solar Energy,* vol. 77, no. 6, pp. 917-930, 2004.

[130] O. Kluth, B. Rech, L. Houben *et al.*, "Texture etched ZnO:Al coated glass substrates for silicon based thin film solar cells," *Thin Solid Films,* vol. 351, no. 1-2, pp. 247-253, 1999.

[131] S. Vepřek, and V. Mareček, "The preparation of thin layers of Ge and Si by chemical hydrogen plasma transport," *Solid State Electronics,* vol. 11, no. 7, pp. 683-684, 1968.

[132] S. Usui, and M. Kikuchi, "Properties of heavily doped GDSi with low resistivity," *Journal of Non-Crystalline Solids,* vol. 34, no. 1, pp. 1-11, 1979.

[133] T. Lule, S. Benthien, H. Keller *et al.*, "Sensitivity of CMOS based imagers and scaling perspectives," *IEEE Transactions on Electron Devices,* vol. 47, no. 11, pp. 2110-2122, 2000.

[134] T. Neidlinger, C. Harendt, J. Gloeckner *et al.*, "Novel device concept for voltage-bias controlled color detection in amorphous silicon sensitized CMOS cameras," *The 1999 MRS Spring Meeting - Symposium B 'Flat-Panel Displays and Sensors-Principles, Materials and Processes'.* pp. 285-290, 1999.

[135] J. A. Theil, "Advances in elevated diode technologies for integrated circuits: Progress towards monolithic instruments," *IEE Proceedings: Circuits, Devices and Systems,* vol. 150, no. 4, pp. 235-249, 2003.

[136] N. Wyrsch, C. Miazza, C. Ballif *et al.*, "Vertical integration of hydrogenated amorphous silicon devices on CMOS circuits," *2005 Materials Research Society Spring Meeting.* pp. 3-14, 2005.

[137] R. Negru, and Y. Bonnassieux, "Amorphous silicon vertical pixel development for high-energy particle detectors: Modelling and technology," *Journal of Non-Crystalline Solids,* vol. 354, no. 19-25, pp. 2619-2622, 2008.

[138] K. Eberhardt, T. Neidlinger, and M. B. Schubert, "Three-color sensor based on amorphous n-i-p-i-n layer sequence," *IEEE Transactions on Electron Devices,* vol. 42, no. 10, pp. 1763-1768, 1995.

[139] N. Moussy, P. Gidon, N. Carriére *et al.*, "A highly reliable Amorphous Silicon photosensor for above IC CMOS image sensor," *2006 International Electron Devices Meeting,* art. no. 4154413, 2006.

[140] T. Nakamura, K. Matsumoto, R. Hyuga *et al.*, "New MOS image sensor operating in a non-destructive readout mode," *International Electron Devices Meeting 1986: IEDM - Technical Digest.* pp. 353-356, 1986.

[141] M. Sugawara, H. Kawashima, F. Andoh *et al.*, "Amplified MOS imager suited for image processing," *Proceedings of the 1994 IEEE International Solid-State Circuits Conference.* pp. 228-229, 1994.

[142] R. H. Nixon, S. E. Kemeny, C. O. Staller *et al.*, "128 x 128 CMOS photodiode-type active pixel sensor with on-chip timing, control, and signal chain electronics," *Charge-Coupled Devices and Solid State Optical Sensors V.* pp. 117-123, 1995.

[143] D. Scheffer, B. Dierickx, and G. Meynants, "Random addressable 2048 × 2048 active pixel image sensor," *IEEE Transactions on Electron Devices,* vol. 44, no. 10, pp. 1716-1720, 1997.

[144] H. B. T. Li, R. H. Franken, J. K. Rath *et al.*, "Structural defects caused by a rough substrate and their influence on the performance of hydrogenated nano-crystalline silicon n-i-p solar cells," *Solar Energy Materials and Solar Cells,* vol. 93, no. 3, pp. 338-349, 2009.

[145] Y. Nasuno, M. Kondo, and A. Matsuda, "Effects of substrate surface morphology on microcrystalline silicon solar cells," *Japanese Journal of Applied Physics, Part 2: Letters,* vol. 40, no. 4 A, 2001.

[146] J. Lu, W. Liu, C. H. M. van der Werf *et al.*, "Above-CMOS a-Si and CIGS Solar Cells for Powering Autonomous Microsystems," *2010 International Electron Devices Meeting,* pp. 31.3.1-31.3.4, 2010.

[147] K. Paik, H. S. Cole, R. J. Saia *et al.*, "Studies on metal/benzocyclobutene (BCB) interface and adhesion," *Journal of Adhesion Science and Technology,* vol. 7, no. 5, pp. 403-415, 1993.

[148] R. E. I. Schropp, K. F. Feenstra, E. C. Molenbroek *et al.*, "Device-quality polycrystalline and amorphous silicon films by hot-wire chemical vapour deposition," *Philosophical Magazine B,* vol. 76, no. 3, pp. 309-321, 1997.

[149] B. W. Ward, J. A. Notte, and N. P. Economou, "Helium ion microscope: A new tool for nanoscale microscopy and metrology," *Journal of Vacuum Science and Technology B,* vol. 24, no. 6, pp. 2871-2874, 2006.

[150] H. B. Li, R. H. Franken, J. K. Rath *et al.*, "Structural defects caused by a rough substrate and their influence on the performance of hydrogenated nano-crystalline silicon n-i-p solar cells," *Solar Energy Materials and Solar Cells,* vol. 93, no. 3, pp. 338-349, 2009.

[151] H. Ali, "Stress-induced parametric shift in plastic packaged devices," *IEEE Transactions on Components Packaging and Manufacturing Technology Part B,* vol. 20, no. 4, pp. 458-462, 1997.

[152] M. Bhushan, A. Gattiker, M. B. Ketchen *et al.*, "Ring oscillators for CMOS process tuning and variability control," *IEEE Transactions on Semiconductor Manufacturing,* vol. 19, no. 1, pp. 10-17, 2006.

[153] H. Van der Graaf, Personal Communication, 2010.

[154] S. Wagner, J. L. Shay, P. Migliorato *et al.*, "$CuInSe_2$/CdS heterojunction photovoltaic detectors," *Applied Physics Letters,* vol. 25, no. 8, pp. 434-435, 1974.

[155] J. L. Shay, S. Wagner, and H. M. Kasper, "Efficient $CuInSe_2$/CdS solar cells," *Applied Physics Letters,* vol. 27, no. 2, pp. 89-90, 1975.

[156] I. Repins, M. A. Contreras, B. Egaas *et al.*, "19.9%-efficient ZnO/CdS/$CuInGaSe_2$ solar cell with 81.2% fill factor," *Progress in Photovoltaics: Research and Applications,* vol. 16, no. 3, pp. 235-239, 2008.

[157] R. A. Mickelsen, and W. S. Chen, "High photocurrent polycrystalline thin-film CdS/$CuInSe_2$ solar cell," *Applied Physics Letters,* vol. 36, no. 5, pp. 371-373, 1980.

[158] K. Mitchell, C. Eberspacher, J. Ermer *et al.*, "Single and tandem junction $CuInSe_2$ cell and module technology," *Twentieth IEEE Photovoltaic Specialists Conference - 1988.* pp. 1384-1389, 1988.

[159] N. Romeo, G. Sberveglieri, L. Tarricone *et al.*, "Preparation and characteristics of $CuGaSe_2$/CdS solar cells," *Applied Physics Letters,* vol. 30, no. 2, pp. 108-110, 1977.

[160] W. S. Chen, J. M. Stewart, W. E. Devaney *et al.*, "Thin film CuInGaSe," *Proceedings of the 23rd IEEE Photovoltaic Specialists Conference.* pp. 422-425, 1993.

[161] W. S. Chen, J. M. Stewart, B. J. Stanbery *et al.*, "Development of thin film polycrystalline $CuIn_{1-x}Ga_xSe_2$ solar cells," *Conference Record of the Nineteenth IEEE Photovoltaic Specialists Conference - 1987.* pp. 1445-1447, 1987.

[162] N. R. Pavaskar, C. A. Menezes, and A. P. B. Sinha, "Photoconductive CdS films by a chemical bath deposition process," *Journal of the Electrochemical Society,* vol. 124, no. 5, pp. 743-748, 1977.

[163] L. Stolt, J. Hedstrom, J. Kessler *et al.*, "ZnO/CdS/$CuInSe_2$ thin-film solar cells with improved performance," *Applied Physics Letters,* vol. 62, no. 6, pp. 597-599, 1993.

[164] W. E. Devaney, W. S. Chen, J. M. Stewart *et al.*, "Structure and properties of high efficiency ZnO/CdZnS/$CuInGaSe_2$ solar cells," *IEEE Transactions on Electron Devices,* vol. 37, no. 2, pp. 428-433, 1990.

[165] W. J. Danaher, L. E. Lyons, and G. C. Morris, "Some properties of thin films of chemically deposited cadmium sulphide," *Solar Energy Materials,* vol. 12, no. 2, pp. 137-148, 1985.

[166] A. M. Gabor, J. R. Tuttle, D. S. Albin *et al.*, "High-efficiency $CuIn_xGa_{1-x}Se_2$ solar cells made from $(In_x,Ga_{1-x})_2Se_3$ precursor films," *Applied Physics Letters,* vol. 65, no. 2, pp. 198-200, 1994.

[167] J. R. Tuttle, M. A. Contreras, T. J. Gillespie *et al.*, "Accelerated publication 17.1% efficient Cu(In,Ga)Se_2-based thin-film solar cell," *Progress in Photovoltaics: Research and Applications,* vol. 3, no. 4, pp. 235-238, 1995.

[168] N. Kohara, T. Negami, M. Nishitani *et al.*, "Preparation of device-quality Cu(In, Ga)Se_2 thin films deposited by coevaporation with composition monitor," *Japanese Journal of Applied Physics, Part 2: Letters,* vol. 34, no. 9 A, 1995.

[169] J. R. Tuttle, M. Contreras, M. H. Bode *et al.*, "Structure, chemistry, and growth mechanisms of photovoltaic quality thin-film Cu(In,Ga)Se_2 grown from a mixed-phase precursor," *Journal of Applied Physics,* vol. 77, no. 1, pp. 153-161, 1995.

[170] M. A. Contreras, B. Egaas, K. Ramanathan *et al.*, "Progress toward 20% efficiency in Cu(In,Ga)Se_2 polycrystalline thin-film solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 7, no. 4, pp. 311-316, 1999.

[171] A. M. Gabor, J. R. Tuttle, M. H. Bode *et al.*, "Band-gap engineering in Cu(In,Ga) Se_2 thin films grown from $(In,Ga)_2Se_3$ precursors," *Solar Energy Materials and Solar Cells,* vol. 41-42, pp. 247-260, 1996.

[172] T. Löher, W. Jaegermann, and C. Pettenkofer, "Formation and electronic properties of the CdS/$CuInSe_2$ (011) heterointerface studied by synchrotron-induced photoemission," *Journal of Applied Physics,* vol. 77, no. 2, pp. 731-738, 1995.

[173] F. Engelhardt, M. Schmidt, T. Meyer *et al.*, "Metastable electrical transport in Cu(In,Ga)Se_2 thin films and ZnO/CdS/Cu(In,Ga)Se_2 heterostructures," *Physics Letters, Section A: General, Atomic and Solid State Physics,* vol. 245, no. 5, pp. 489-493, 1998.

[174] D. Schmid, M. Ruckh, F. Grunwald *et al.*, "Chalcopyrite/defect chalcopyrite heterojunctions on the basis of $CuInSe_2$," *Journal of Applied Physics,* vol. 73, no. 6, pp. 2902-2909, 1993.

[175] U. Rau, "Tunneling-enhanced recombination in Cu(In, Ga)Se_2 heterojunction solar cells," *Applied Physics Letters,* vol. 74, no. 1, pp. 111-113, 1999.

[176] U. Rau, and H. W. Schock, "Electronic properties of Cu(In,Ga)Se_2 heterojunction solar cells-recent achievements, current understanding, and future challenges," *Applied Physics A: Materials Science and Processing,* vol. 69, no. 2, pp. 131-147, 1999.

[177] S. Siebentritt, M. Igalson, C. Persson *et al.*, "The electronic structure of chalcopyrites - Bands, point defects and grain boundaries," *Progress in Photovoltaics: Research and Applications,* vol. 18, no. 6, pp. 390-410, 2010.

[178] M. Morkel, L. Weinhardt, B. Lohmüller *et al.*, "Flat conduction-band alignment at the CdS/$CuInSe_2$ thin-film solar-cell heterojunction," *Applied Physics Letters,* vol. 79, no. 27, pp. 4482-4484, 2001.

[179] U. Rau, and M. Schmidt, "Electronic properties of ZnO/CdS/Cu(In,Ga)Se_2 solar cells - Aspects of heterojunction formation," *Thin Solid Films,* vol. 387, no. 1-2, pp. 141-146, 2001.

[180] K. Granath, M. Bodegård, and L. Stolt, "Effect of NaF on Cu(In, Ga)Se_2 thin film solar cells," *Solar Energy Materials and Solar Cells,* vol. 60, no. 3, pp. 279-293, 2000.

[181] D. Rudmann, G. Bilger, M. Kaelin *et al.*, "Effects of NaF coevaporation on structural properties of Cu(In,Ga)Se_2 thin films," *Thin Solid Films,* vol. 431-432, pp. 37-40, 18, 2003.

[182] J. F. Guillemoles, L. Kronik, D. Cahen *et al.*, "Stability Issues of Cu(In,Ga)Se_2-Based Solar Cells," *Journal of Physical Chemistry B,* vol. 104, no. 20, pp. 4849-4862, 2000.

[183] O. Matsushima, K. Miyazaki, M. Takaoka *et al.*, "A high-sensitivity broadband image sensor using $CuInGaSe_2$ thin films." IEDM 2007.

[184] J. H. Scofield, A. Duda, D. Albin *et al.*, "Sputtered molybdenum bilayer back contact for copper indium diselenide-based polycrystalline thin-film solar cells," *Thin Solid Films,* vol. 260, no. 1, pp. 26-31, 1995.

[185] J. Strong, "On the cleaning of surfaces," *Review of Scientific Instruments,* vol. 6, no. 4, pp. 97-98, 1935.

[186] A. Broniatowski, "Multicarrier trapping by copper microprecipitates in silicon," *Physical Review Letters,* vol. 62, no. 26, pp. 3074-3077, 1989.

[187] M. A. Nicolet, "Diffusion barriers in thin films," *Thin Solid Films,* vol. 52, no. 3, pp. 415-443, 1978.

[188] J. P. McVittie, "Plasma charging damage: an overview," Proceedings of the 1996 1st International Symposium on Plasma Process-Induced Damage, P2ID. pp. 7-10.

[189] C. T. Gabriel, and M. G. Weling, "Gate oxide damage reduction using a protective dielectric layer," *Electron Device Letters, IEEE,* vol. 15, no. 8, pp. 269-271, 1994.

[190] S. Wolf, and R. N. Tauber, *Silicon processing for the VLSI era. 2, Process integration*, Sunset Beach, Calif.: Lattice Press, 1990.

[191] F. Kessler, and D. Rudmann, "Technological aspects of flexible CIGS solar cells and modules," *Solar Energy,* vol. 77, no. 6, pp. 685-695, 2004.

[192] M. Bodeg Árd, K. Granath, and L. Stolt, "Growth of Cu(In,Ga)Se_2 thin films by coevaporation using alkaline precursors," *Thin Solid Films,* vol. 361, pp. 9-16, 2000.

[193] S. Nishiwaki, T. Satoh, Y. Hashimoto *et al.*, "Preparation of Cu(In,Ga)Se_2 thin films at low substrate temperatures," *Journal of Materials Research,* vol. 16, no. 2, pp. 394-399, 2001.

[194] S. M. Hu, "Stress-related problems in silicon technology," *Journal of Applied Physics,* vol. 70, no. 6, 1991.

[195] C. Y. Shi, Y. Sun, Q. He *et al.*, "Cu(In,Ga)Se_2 solar cells on stainless-steel substrates covered with ZnO diffusion barriers," *Solar Energy Materials and Solar Cells,* vol. 93, no. 5, pp. 654-656, 2009.

[196] A. L. Patterson, "The Scherrer Formula for X-Ray Particle Size Determination," *Physical Review,* vol. 56, no. 10, pp. 978, 1939.

[197] J. I. Langford, and A. J. C. Wilson, "Scherrer after sixty years: A survey and some new results in the determination of crystallite size," *Journal of Applied Crystallography,* vol. 11, no. 2, pp. 102-113, 1978.

[198] J. Lu, W. Liu, A. Y. Kovalgin *et al.*, "Materials Characterization of CIGS solar cells on Top of CMOS chips," *2011 MRS Spring Meeting*, in printing.

[199] J. A. Thornton, "Influence of appratus geometry and deposition conditions on the structure and topography of thick sputtered coatings," *J Vac Sci Technol,* vol. 11, no. 4, pp. 666-670, 1974.

[200] R. F. Bunshah, "Structure/Property relationships in evaporated thick films and bulk coatings," *J Vac Sci Technol,* vol. 11, no. 4, pp. 633-638, 1974.

[201] D. Abou-Ras, R. Caballero, C. A. Kaufmann *et al.*, "Impact of the Ga concentration on the microstructure of $CuIn_{1-x}Ga_xSe_2$," *physica status solidi (RRL) – Rapid Research Letters,* vol. 2, no. 3, pp. 135-137, 2008.

[202] M. A. Contreras, M. J. Romero, and R. Noufi, "Characterization of $Cu(In,Ga)Se_2$ materials used in record performance solar cells," *Thin Solid Films,* vol. 511-512, pp. 51-54, 2006.

[203] T. Wada, N. Kohara, T. Negami *et al.*, "Chemical and structural characterization of $Cu(In, Ga)Se_2$/Mo interface in $Cu(In, Ga)Se_2$ solar cells," *Japanese Journal of Applied Physics, Part 2: Letters,* vol. 35, no. 10 PART A, 1996.

[204] C. A. Kaufmann, A. Neisser, R. Klenk *et al.*, "Transfer of $Cu(In,Ga)Se_2$ thin film solar cells to flexible substrates using an in situ process control," *Thin Solid Films,* vol. 480-481, pp. 515-519, 2005.

Conclusies en aanbevelingen

Conclusies

Dit proefschrift gaat over Energy Harvesting, een van de meest prominente onderwerpen in de hedendaagse elektrotechniek, zowel in de industrie als in de wetenschap. Energy Harvesting omvat een veelvoud aan technieken voor het winnen van omgevingsenergie. Het kan beschouwd worden als een vorm van elektronisch sprokkelen, de energie wordt opgewekt uit alomtegenwoordige bronnen die anderszins niet benut worden. In deze tekst blijven we de Engelstalige term gebruiken. De techniek vormt de basis voor autonome draadloze netwerken, een van de essentiële onderdelen voor het zogeheten 'ubiquitous computing' (alomtegenwoordige computers). Dit laatste is een ideaal waarin computerkracht uiterst fijnmazig verweven wordt met de omgeving zodat deze optimaal benut kan worden.

Er zijn verschillende manieren om succesvol Energy Harvesting te bedrijven, alle met hun eigen voor- en nadelen. In dit proefschrift richten we ons op monolithische integratie van een Energy Harvester bovenop CMOS chips. Deze structuren zijn gemaakt met behulp van met CMOS compatibele nabewerkingsstappen. Twee verschillende methoden zijn onderzocht.

Hoofdstuk 2 beschrijft de eerste methode, dit is een geïntegreerde elektromagnetische Energy Harvester. Deze structuur wint energie uit mechanische vibraties. Computersimulaties hebben aangetoond dat met een elektromagnetische EH een vermogen op het niveau van microwatts opgewekt kan worden, dit komt goed overeen met experimentele resultaten van andere onderzoekers. Vanwege een gebrek aan zekere essentiële apparatuur en vanwege complicaties met de frequentie afstemming (zie pagina 28) is de uiteindelijke uitvoering van dit experiment achterwege gelaten.

Hoofdstuk 3 tot en met 5 behandelen de tweede uitvoeringsvorm van een EH. Deze bestaat uit een geïntegreerde zonnecel op het oppervlak van een CMOS chip. De CMOS vervaardiging is volledig conventioneel. Ook de technieken gebruikt voor het fabriceren van de zonnecel zijn volledig ongewijzigd ten opzichte van niet-geïntegreerde systemen. De geïntegreerde zonnecel wordt gebruikt om zonlicht om te zetten in elektrische energie, die

vervolgens wordt doorgegeven aan de onderliggende CMOS schakeling. Aan de hand van een uitvoerig onderzoek is besloten de zonnecellen te vervaardigen uit twee verschillende materialen, te weten amorf silicium (a-Si) en koper-indium-gallium-selenide (CIGS).

Compatibiliteit met CMOS

Bij de integratie van een zonnecel op een CMOS chip worden twee doelen tegelijkertijd nagestreefd: de zonnecel moet goed functioneren en de CMOS chip moet onveranderd blijven werken. Dit werpt een aantal uitdagingen op.

Een aantal mogelijke, nadelige effecten van de nabewerking op het CMOS IC worden opgesomd in sectie 1.2.4. Sectie 3.1.3 toont aan dat deze effecten kunnen worden vermeden, een belangrijke voorwaarde hiervoor is het gebruik van een goede passivatielaag aan beide zijden van de chip. Voor de experimentele verificatie zijn drie verschillende CMOS chips gebruikt: de Timepix chip (gemaakt in 0.25 μm technologie, Al backend), de Ring Oscillator (in 0.18 μm technologie met eveneens een Al back-end) en de PCM teststructuren van een Cu back-end 0.13 μm chip. Door de chips elektrisch te karakteriseren voor en na de nabewerking wordt een goed beeld verkregen van het effect van de behandeling en de compatibiliteit op drie verschillende niveaus: van een enkele component (een MOS condensator of een MOSFET), via een losse schakeling (de Ring Oscillator) naar een complex CMOS IC (de Timepix chip).

Voor a-Si zonnecellen vormt schade veroorzaakt door oplading uit plasma's de grootste bedreiging. Plasma's zijn noodzakelijk voor bijna alle processtappen, hierbij kan lading worden opgepikt die het gate diëlektricum van transistoren kan beschadigen. Een ander risico is de aanwezigheid van dunne zilverlagen, benodigd om de efficiëntie van de zonnecel te verbeteren. Metaalionen zoals zilver kunnen een ernstige bedreiging vormen voor de werking van CMOS transistoren. Beide risico's kunnen ingeperkt worden door het gebruik van een goede passivatielaag. De effectiviteit van de gepresenteerde lagen is experimenteel aangetoond.

Voor de CIGS zonnecellen is het grootse probleem de hoge temperatuur die nodig is voor de fabricage van het CIGS materiaal. Temperaturen van 320 tot 550 ºC zijn gebruikelijk, hoe hoger de temperatuur hoe beter de zonnecel werkt. Dergelijke temperaturen zijn echter bijzonder schadelijk voor de

CMOS chips, met name voor de metaalverbindingen in het bovenste deel van de chip. Een serie experimenten is uitgevoerd om te onderzoeken wat de hoogst haalbare temperatuur is voor CMOS chips, hieruit blijkt dat de de temperatuur beneden de 425 ºC moet blijven.

Ook mechanische stress kan een bedreiging vormen voor bepaalde onderdelen van de CMOS chip zoals het isolatiemateriaal in het interconnect. De CIGS lagen die bovenop de CMOS chip worden gegroeid kunnen de onderliggende laag fysiek beschadigen. Mechanische stress kan ook veroorzaakt worden door de hoge temperatuur. Bij een temperatuur van 425 °C is gebleken dat integratie van zonnecellen op de achterkant van de chip wel succesvol gedaan kan worden, maar op de voorkant is dit niet mogelijk. Bij dit laatste ontstaat een verminderde werking van de CMOS structuren door de invloed van mechanische stress.

Een bijkomend probleem is het risico van contaminatie met natriumionen, Na wordt gebruikt voor het verbeteren van de werking van het CIGS halfgeleidermateriaal. Om de natriumionen tegen te houden is een goede barrièrelaag nodig tussen het CIGS materiaal en het CMOS substraat. De werking van de juiste barrièrelaag is experimenteel geverifieerd met behulp van de verschillende test chips.

Samenvattend kan gesteld worden dat, mits geschikte barrièrelagen worden gebruikt, het mogelijk is om CIGS zonnecellen te integreren op de achterkant van CMOS chips indien de temperatuur beneden de 425 °C blijft.

Efficiëntie en functionaliteit van geïntegreerde zonnecellen

Het type zonnecellen dat hier is bestudeerd wordt normaal gefabriceerd op natronkalk-glas substraten. Wanneer de zonnecel op een CMOS chip wordt gemaakt eisen we dat de efficiëntie en de fractie functionele zonnecellen (van het totaal) gelijk blijven. Dat is niet triviaal, de twee belangrijkste veroorzakers van problemen zijn het oppervlakteprofiel (de chip is minder vlak dan een kaal substraat) en de verminderde hechting van het zonnecel materiaal op de CMOS chip.

Conventionele substraten hebben een oppervlakteprofiel met minder dan 50 nm variatie in hoogte. Bij een CMOS chip kan dit variëren van enkele honderden nanometers tot meer dan 1.5 μm, afhankelijk van de laatste

processtappen die zijn gebruikt. Natronkalk-glas substraten bestaan uit amorf SiO_2, het oppervlak van CMOS chips is bedekt met PECVD SiO_2.

Onze experimenten hebben aangetoond dat het oppervlakte profiel van CMOS chips een nadelig effort heeft op de fractie functionele a-Si zonnecellen, voor CIGS zonnecellen is de efficiëntie aangetast. Conventionele CIGS processen leiden niet tot een goede hechting op CMOS substraten.

In dit proefschrift worden een aantal technologische aanpassingen voorgesteld om de functionaliteit en de efficiëntie van de geïntegreerde zonnecellen te verbeteren. Door het gebruik van een 3 μm dikke planarisatielaag van BCB voorafgaand aan het maken van de a-Si zonnecel wordt een efficiëntie van 7.15% bereikt terwijl 92% van de zonnecellen functioneel bleek. Voor de CIGS zonnecellen is een efficiëntie van 8.4% behaald, 84% van de structuren was functioneel. Om deze resultaten te bereiken is een 10 nm dunne titanium hechtingslaag toegevoegd aan het proces. Voor beide type zonnecellen zijn de uiteindelijke resultaten vergelijkbaar met wat doorgaans op conventionele glazen substraten bereikt wordt.

Dit proefschrift toont aan dat de beide typen zonnecellen succesvol kunnen worden toegepast voor Energy Harvesting. Bij AM 1.5 belichting kan een vermogen van 7 mW/cm^2 opgewekt worden. Bij binnenshuis-omstandigheden kan een vermogen van 0.6~6 $\mu W/cm^2$ gegenereerd worden, afhankelijk van de afstand tussen de lichtbron en de Energy Harvester en van de lichtintensiteit.

Vergelijking van de verschillende technieken

We hebben drie verschillende technieken gepresenteerd voor het maken van een Energy Harvester. Dat zijn de elektromagnetische structuur waarbij energie wordt opgewekt uit mechanische vibraties, een geïntegreerde a-Si zonnecel en een geïntegreerde CIGS zonnecel.

Ondanks dat het moeilijk is om de EM structuur correct af te stemmen op de frequentie van de energiebron kan deze methode niet worden uitgesloten. In sommige gevallen is er geen andere energiebron voorhanden, ook wanneer er sprake is van vibraties met een vaste trillingsfrequentie heeft de EM Energy Harvester de voorkeur.

Twee verschillende soorten zonnecellen zijn geïntegreerd op CMOS chips. De zonnecellen gemaakt van a-Si hebben minder nadelige invloed op de

CMOS chips, de CIGS gebaseerde zonnecellen hebben echter een hogere efficiëntie (bij AM 1.5 belichting). Bij zwakke belichting, met een intensiteit van minder dan 1 mW/cm^2 , is het mogelijk dat de a-Si zonnecel een hogere efficiëntie heeft dan de CIGS zonnecel [1].

Er zijn drie situaties waarin CIGS zonnecellen de voorkeur genieten.

Wanneer het interconnect (of 'back-end') volledig van koper is gemaakt, zonder enig gebruik van aluminium; dit soort chips kan een hogere temperatuur aan. Als het CIGS proces bij meer dan 450 ºC wordt uitgevoerd zal dit leiden tot een efficiëntie van meer dan 15%. Of de CMOS chips (met volledig Cu back-end) dit kunnen doorstaan moet experimenteel worden aangetoond.

Wanneer de zonnecel wordt gebruikt in direct zonlicht. Zelfs CIGS zonnecellen gemaakt bij 400 ºC vertonen dan nog een betere efficiëntie dan de beste a-Si zonnecellen (maximaal 10%).

Wanneer de Energy Harvester wordt gebruikt in een omgeving met hoog stralingsniveau, bijvoorbeeld in de ruimte. CIGS hebben een uitzonderlijke stralingstolerantie en zijn in dit soort situaties stabieler dan a-Si.

In alle andere gevallen is het beter om een zonnecel te vervaardigen uit a-Si. Dit materiaal is ook verreweg het meest gebruikt in de PV industrie. Daarnaast is silicium, het basismateriaal, een van de meest bestudeerde en goed gekarakteriseerde materialen in de IC industrie. Samengevat kan gesteld worden: als het met silicium gemaakt kan worden, maak het dan met silicium.

Aanbevelingen

Dit proefschrift gaat over de eerste, initiële experimenten met op CMOS geïntegreerde zonnecellen voor Energy Harvesting. Verder onderzoek naar de haalbaarheid van dergelijke hybride apparaten moet zich toespitsen op de volgende onderwerpen.

1) Het maken van een goede elektrische verbinding tussen de zonnecel en de onderliggende CMOS chip. Voor zonnecellen op de voorkant van de chip zijn verticale geleidende verbindingen (zogeheten via's) door de passivatielaag benodigd. Voor integratie op de achterkant van

[1] Volgens de literatuur beschikbaar op het moment van schrijven [23, 24, 105]

de chip moeten deze via's dwars door de gehele wafer worden gemaakt.

2) Het testen van de efficiëntie van de zonnecel bij gebruik binnenshuis. Hiervoor kunnen twee verschillende meetmethoden gevolgd worden[1]. Ten eerste kan gemeten worden bij een AM 1.5 spectrum met een verlaagde intensiteit. Met behulp van grijsfilters (Neutral Density of ND filters) kan de zonnecel gekarakteriseerd worden van 100% tot aan 0.1% belichting, het spectrum komt overeen met de normale AM 1.5 belichting, alleen de intensiteit is aangepast. Ten tweede kunnen de zonnecellen belicht worden met een fluorescentielamp zoals die normaal binnenshuis gebruikt worden. Om de efficiëntie te kunnen bepalen is dan een gekalibreerde referentiedetector nodig.
3) Het in overeenstemming brengen van de spanning die door de zonnecel afgegeven wordt en de spanning die voor het CMOS IC benodigd is. De behaalde spanningen zijn maximaal 0.4 V en 0.7 V voor respectievelijk de CIGS en de a-Si zonnecel. Voor veel CMOS ICs is de benodigde voedingsspanning minstens 1 V. De opgewekte spanningen moeten verhoogd worden. Dit kan bereikt worden door meerdere zonnecellen in serieschakeling aan te sluiten, hiervoor moeten nieuwe fabricagestappen ontwikkeld worden. Een andere mogelijkheid is het maken van zonnecellen met meerdere, gestapelde actieve lagen. Dit vereist een groot aantal technologische aanpassingen in het integratieproces.
4) Voor een volledig Energy Harvesting systeem moeten structuren voor vermogensbeheersing en energieopslag ontwikkeld worden. Het is belangrijk dat deze structuren uiterst efficiënt zijn. De vermogensbeheersing kan onderdeel zijn van het CMOS IC. De opslag kan gedaan worden met zogeheten super condensators.
5) Verbetering van de efficiëntie bij binnenshuis-belichting. De meeste zonnecellen zijn geoptimaliseerd voor gebruik in de felle zon (de standaard AM 1.5 belichting). Er is nog maar weinig onderzoek gedaan naar de werking van zonnecellen bij omgevingslicht, zo is er

[1] Naar aanleiding van correspondentie met Prof. Schropp, maart 2011.

geen breed geaccepteerde standaard test methode voor dit soort belichtingssituatie. Een belangrijke eerste stap is het ontwikkelen van de benodigde procedures. Daarna denken we aan twee verschillende manieren om de efficiëntie te verbeteren. Ten eerste het aanpassen van de bandgap van het halfgeleidermateriaal waaruit de zonnecel gemaakt is, zodat deze goed aansluit bij het lichtspectrum binnenshuis. Voor a-Si zonnecellen kan dit bereikt worden door aanpassen van de waterstofconcentratie in het materiaal, in het geval van CIGS zonnecellen kan een vergelijkbaar effect bereikt worden door aanpassing van de hoeveelheid Ga die opgenomen is in de laag. Een tweede methode voor het bereiken van een hogere efficiëntie in omgevingslicht is het verbeteren van de kwaliteit van het bovenste gedeelte van de zonnecel. Het licht binnenshuis heeft een uiterst lage intensiteit en een hogere golflengte dan zonlicht en zal dus niet veel verder doordringen dan in de bovenste laag van ongeveer 100 nm. De kwaliteit aldaar is derhalve cruciaal.

6) Het maken van elementen voor een draadloos netwerk op basis van CMOS chips die daadwerkelijk worden gevoed met geïntegreerde zonnecellen. Het aantonen van de werking van dit soort elementen bij verschillende belichtingssituaties.

List of Publications

1. J. Lu, W. Liu, A. Y. Kovalgin, Y. Sun and J. Schmitz, "*Integration of solar cells on top of CMOS chips Part II: CIGS Solar cells*," Accepted for publication by IEEE Transaction on Electron Devices, 2011
2. J. Lu, C. H. M. Van Der Werf, A. Y. Kovalgin, R. E. I. Schropp, and J. Schmitz, "*Integration of solar cells on top of CMOS chips Part I: a-Si Solar cells*," Accepted for publication by IEEE Transaction on Electron Devices, 2011
3. J. Lu, W. Liu, A. Y. Kovalgin Y. Sun and J. Schmitz, "*Materials Characterization of CIGS solar cells on Top of CMOS chips*," *2011 MRS Spring Meeting*.
4. V. M. Blanco Carballo, M. Fransen, H. Van Der Graaf, J. Lu, and J. Schmitz, "*A CMOS compatible Microbulk Micromegas-like detector using silicon oxide as spacer material*," Nuclear Instruments and Methods in Physics Research, vol. 629, no. 1, pp. 118-122, 2011
5. J. Lu, W. Liu, C. H. M. Van Der Werf, A. Y. Kovalgin, Y. Sun, R. E. I. Schropp, and J. Schmitz, "*Above-CMOS a-Si and CIGS solar cells for powering autonomous microsystems*," 2010 IEEE International Electron Devices Meeting, IEDM 2010. pp. 31.3.1-31.3.4
6. J. Lu, A. Y. Kovalgin and J. Schmitz, "*Influence of passivation process on chip performance*," Proceedings of the 12th Annual Workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE2009), 26-27 Nov 2009, Veldhoven, The Netherlands. pp. 542-544. ISBN 978-90-73461-62-8.
7. J. Lu, T. Conka Nurdan, K. Nurdan, A.H. Walenta, "*Angular effects on the operation of an Anger camera in the Compton camera application*", under preparation for Nuclear Instruments and Methods in Physics Research.

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